Instruction Manual

Tektronix

TMS568
MPC85XX Microprocessor Software Support

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www.tektronix.com

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Preface

This instruction manual contains specific information about the TMS568 MPC85XX microprocessor support product and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS568 MPC85XX microprocessor support product was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of logic analyzer online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the target system
- Setting up the logic analyzer to acquire data from the target system
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles microprocessor cycles into instruction mnemonics and cycle types.
- The phrase “basic operations” refers to the logic analyzer online help, or the user manual that covers the basic operations of the microprocessor support.
- The phrase “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Contacting Tektronix

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*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains information on the TMS568 MPC85XX microprocessor support product and information on connecting your logic analyzer to your target system.

Support Package Description

The TMS568 MPC85XX microprocessor support product displays disassembled data from systems based on MPC8540/8560. The support package allows you to acquire microprocessor cycles with minimal impact on the environment of the system.

The TMS568 MPC85XX microprocessor support product contains five support packages that have their own setup software and disassemblers. A description of each support package is listed here:

- 85XXDDR acquires DDR commands and DDR reads or DDR writes.
- 85XXDDR_RW acquires commands and both DDR reads and writes simultaneously.
- 85XXLB acquires the SDRAM and GPCM cycles on the local bus.
- 85XXLB_ALT acquires the SDRAM and GPCM bus cycles from 85XX local bus interface. This support package can be used with reference boards having alternate channel assignment. Refer to the channel assignment section for details.
- 85XXLB_ADS acquires the SDRAM and GPCM bus cycles from 85XX local bus interface. This support package is compatible with Motorola ADS reference board channel assignment.

Disassembly Support

The disassembler decodes information from the DDR and local bus interfaces.

To use this support package efficiently refer to the following documents:

- *MPC8540 INTEGRATED PROCESSOR PRELIMINARY USER'S MANUAL, {Motorola, MPC8540xxxx 3/2002, Rev.1.3}*
- *MPC8560 PowerQUICC III INTEGRATED COMMUNICATION PROCESSOR PRELIMINARY USER'S MANUAL, {Motorola MPC8560xxxx, 1/2003, Rev.2.0}*
- *JEDEC STANDARD, DDR SDRAM Specification, JESD79, Release 2, May 2002.*

- *NEX_SPA (Sample point analyzer), Nexus technologies(www.bus-boards.com).*

Logic Analyzer Software Compatibility

The label on the microprocessor support CD-ROM states which version of logic analyzer software this support package is compatible with.

Logic Analyzer Configuration

The TMS568 product allows a choice of required minimum module configurations.

Module Requirements

Table 1–1 lists the minimum module requirements for the TMS568 MPC85XX microprocessor support product.

Table 1–1: Module requirements

Support package	Module requirements
85XXDDR	One TLA7Ax4 450 MHz, 136-channel module
85XXDDR_RW	Two TLA7Ax4 450 MHz, 136-channel modules in merged configuration
85XXLB	One TLA7N2 module 200 MHz, 68-channel module
85XXLB_ALT	One TLA7N3 module 200 MHz, 102-channel module
85XXLB_ADS	TLA7Ax2 module 235 MHz state speed, 68-channel module

Probe Requirements

Table 1–2 lists the probe requirements for the TMS568 MPC85XX microprocessor support product.

Table 1–2: Probe requirements

Support package	Probe requirements
85XXDDR	Four P6860 probes
85XXDDR_RW	Eight P6860 probes
85XXLB	Two P6434 probes
85XXLB_ALT	Three P6434 probes
85XXLB_ADS	Two P6860 probes

Requirements and Restrictions

Review the electrical specifications in the *Specifications* section on page 4–1 in this manual as they pertain to your target system, as well as the following descriptions of TMS568 MPC85XX microprocessor support product requirements and restrictions.

Hardware Reset

If a hardware reset occurs in your target system during an acquisition, the application disassembler might acquire an invalid sample.

Clock Rate

The maximum clock rate for local bus is 166 MHz and for DDR–SDRAM is 200 MHz.

Setup/Hold Time Adjustments

The DDR reads and writes have different timings. The DQS and data are edge aligned for reads and center aligned for writes. 85XXDDR support package has default setup hold timings valid for reads. To capture write data accurately or if the DDR SDRAM timings are different, you need to adjust the setup/hold timing values. This can be done either manually or using a tool.

To manually adjust setup/hold, trigger on a read or a write cycle appropriately. Then, in the MagniVu, find the data valid window for DDR data with reference to the clock edge. Select setup/hold timings in custom clocking option, in such a way that the setup/hold window falls at the center of the data valid window.

To assist in this operation, a software tool called DDR Sample Point Analysis Software (NEX-SPA) is available from Nexus Technology, Inc (a Tektronix Embedded System Tools Partner). The tool and a user guide can be downloaded from their web site, www.busboards.com.

Table 1–3 lists the setup/hold time requirements for the different support packages. For correct acquisition, the target system must provide a data valid window meeting these requirements.

Table 1–3: Setup/Hold time requirements for the MPC85XX product

Support package name	Logic analyzer/ module	Setup time	Hold time
85XXDDR	One TLA7Ax4 450 MHz, 136–channel module	750 ps	0 ps
85XXDDR_RW	Two TLAAx4 450 MHz, 136–channel modules in merged configuration	750 ps	0 ps
85XXLB	One TLA7N2 module 200 MHz, 68–channel module	2.5 ns	0 ps

Table 1-3: Setup/Hold time requirements for the MPC85XX product (Cont.)

Support package name	Logic analyzer/ module	Setup time	Hold time
85XXLB_ALT	One TLA7N3 module 200 MHz, 102-channel module	2.5 ns	0 ps
85XXLB_ADS	TLA7Ax2 module 235 MHz state speed, 68-channel module	2.5 ns	0 ps

Nonintrusive Acquisition

Acquiring microprocessor cycles is nonintrusive to the target system. The TMS568 MPC85XX microprocessor support product does not intercept, modify, or present signals back to the system under test.

Limitations of the Support

The TMS568 MPC85XX microprocessor support product does not support the following:

- Local Bus SDRAM extended CAS Latency “4,5,6,7”.
- UPM cycles.

Connecting the Logic Analyzer to a Target System

You can use the channel probes to make the connections between the logic analyzer and your target system.

To connect the probes to the target system as described in the TMS568 MPC85XX microprocessor support product channel assignment, follow the steps:

1. Power off your target system. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the target systems, probes, and the logic analyzer module in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the target system.

2. Place the target system on a horizontal, static-free surface.

3. Use tables 3–87 through 3–126 starting on page 3–55 to connect the channel probes to the necessary signals in the target system.

A probe adapter (NEX–DDRHS) that connects the Logic Analyzer to a JEDEC standard DDR–SDRAM slot is available from Nexus Technology Inc. (a Tektronix Embedded Systems Tools Partner). TMS568 DDR–SDRAM supports are compatible with this probe adapter. When using this probe adapter, an automatic dequeue feature is available only if the Debug signals are routed through the ECC pins.

Contact your Tektronix representative if you require any assistance regarding the probe adapter.

Labeling P6434 and P6860 Probes

The TMS568 MPC85XX microprocessor support product relies on the channel mapping and labeling scheme for the P6860 and P6434 Probes. Apply labels, using the instructions described in the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction* manual and *P6434 Logic Analyzer Probes Instruction* manual.

Operating Basics

Setting Up the Support

This section provides information on how to set up the software support and covers the following topics:

- Installing the support software
- Support package setups
- Clocking options

The information in this section pertains to the specific operations and functions of the TMS568 MPC85XX microprocessor support product on a Tektronix logic analyzer.

Before you acquire and display disassembled data, you need to load the support package and specify the setups for clocking and triggering as described in the logic analyzer online help under “Microprocessor support”. The support package provides default values for each of these setups, but you can change the setups as needed.

Installing the Support Software

***NOTE**. Before you install any software, it is recommended you verify that the microprocessor support software is compatible with the logic analyzer software.*

To install the TMS568 MPC85XX microprocessor support product on your Tektronix logic analyzer, follow these steps:

1. Insert the CD-ROM in the CD drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the CD-ROM. A copy of the instruction manual is available on the CD-ROM.

To remove or uninstall software, follow the above instructions and select Uninstall. You need to close all windows before you uninstall any software.

The TMS568 MPC85XX microprocessor support product installs five different support packages.

Support Package Setups

The TMS568 MPC85XX microprocessor support product installs five support packages that have their own setup software and disassemblers. A description of each support package is listed here:

- 85XXDDR: This support package acquires DDR commands and DDR reads or DDR writes.
- 85XXDDR_RW: This support package acquires commands and both DDR reads and writes simultaneously.
- 85XXLB: This support package acquires the SDRAM and GPCM cycles on the local bus.
- 85XXLB_ALT: This support package acquires SDRAM and GPCM bus cycles from 85XX local bus interface. Use this package with reference boards that have alternate channel assignment. Refer to the channel assignment section for more details.
- 85XXLB_ADS: This support package is compatible with Motorola ADS reference board channel assignment. This support package acquires SDRAM and GPCM bus cycles from 85XX local bus interface.

The TMS568 MPC85XX microprocessor support product adds these five selections to the “Load Support Package” dialog box, under the File pulldown menu.

Clocking Options

A special custom clocking program is loaded into the module every time you load one of the 85XXDDR, 85XXDDR_RW, 85XXLB, 85XXLB_ALT or 85XXLB_ADS support packages from the TMS568 MPC85XX microprocessor support product. Each support package offers different clocking options. You may use the default clocking option or choose an alternate by clicking the “More...” button in the logic analyzer setup window.

85XXDDR and 85XXDDR_RW Support Packages

The software provides three custom clocking options for the 85XXDDR and 85XXDDR_RW support packages.

DDR Clocking. Permits selection between DDR clocks (MCK0, MCK1, MCK2) and chip selects (MCS0 or/and MCS1) to acquire DDR data. Select the approriate option from the following:

DDR MCK0; MCS0~ only active (default)
DDR MCK0; MCS0~ and MCS1~active
DDR MCK1; MCS0~ only active

DDR MCK1; MCS0~ and MCS1~active
DDR MCK2; MCS0~ only active, or
DDR MCK2; MCS0~ and MCS1~active

Clock Mode. Select the type of data acquisition.

Selective Clocking (default)
This mode reduces the number of idle cycles stored by the acquisition card to optimally use the acquisition memory. Data is stored whenever MRAS~ or MCAS~ is asserted, along with CS0~ or CS1~. After every assertion of MCAS~, additional 17 samples are taken on every DDR Clock edge. If MCAS~ and ChipSelect are asserted during these 17 samples, the count is reset.

***NOTE**. This mode does not work if the DDR target uses ChipSelect CS3~ or CS4~ to enable the DDR memory.*

Every DDR Clock Edge
This mode causes the acquisition card to store data on every Rising and Falling edge of the selected DDR SDRAM clock.

Refresh Cycles. Select one of the following options to either acquire or not acquire refresh cycles.

Do not acquire (default) – This selection does not acquire refresh cycles.
Acquire – This selection acquires refresh cycles.

85XXLB, 85XXLB_ALT, and 85XXLB_ADS Support Packages

The software provides four custom clocking options for the 85XXLB, 85XXLB_ALT, and 85XXLB_ADS support packages.

Debug Mode. Acquires data when Debug Signals are available or not available.

Disabled (default)
Enabled

Clock Mode. Select the type of data acquisition.

Selective Clocking (default)
This mode reduces the number of idle cycles stored by the acquisition card to optimally use acquisition memory.

Every LB Clock Falling-Edge
This mode causes the acquisition card to store data on every falling edge of the selected local bus clock.

SDRAM: CAS Latency. Select SDRAM CAS Latency as one of the following:

One (default)
Two
Three

SDRAM: Port Size. Select the SDRAM Port Size as one of the following:

16 bit (default)
8 bit or 32 bit

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. The following information covers these topics and tasks:

- Acquiring data
- Changing how data is displayed
- Viewing cycle type labels
- Viewing disassembled data in various display formats

Acquiring Data

The TMS568 MPC85XX microprocessor support product installs five different support packages: 85XXDDR, 85XXDDR_RW, 85XXLB, 85XXLB_ALT, and 85XXLB_ADS.

Once you load the support package, choose a clocking mode, adjust the logic analyzer setup/hold window if required, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to the information on basic operations in your logic analyzer online help.

Changing How Data is Displayed

Common fields and features allow you to further modify displayed data to fit your needs. You can make common and optional display selections in the disassembly property page.

You can make selections unique to the support package from the TMS568 MPC85XX microprocessor support product to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles

Optional Display Selections

Table 2–1 shows the disassembly display options for 85XXDDR, 85XXDDR_RW, 85XXLB, 85XXLB_ALT, and 85XXLB_ADS support packages.

Table 2–1: Logic analyzer disassembly display options

Option	Selections
Show	Hardware (default) Software Control Flow Subroutine
Highlight	Hardware (default) Software Control Flow Subroutine
Disassemble Across Gaps	Yes No (default)

Microprocessor Specific Fields for the 85XXDDR Support Package

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways.

Show DESELECT cycles. Choose from the following selections depending on whether you want to see the DESELECT cycles in the Listing Window.

Yes (default)
No

Show all data?. Choose among the following selections depending on whether you wish to see Valid Data in the Listing Window.

Yes (default)
No

Processor used. Choose between the following microprocessors.

MPC8540 (default)
MPC8560

Debug Signals. Choose among the following selections depending on where the debug signals are available.

Disabled (default)
Debug signals on MSRCID
Debug signals on ECC

Valid Cycles. Choose among the following selections depending on whether you are acquiring DDR reads/writes.

Reads (default)
Writes

DDR configuration. Choose among the following selections depending on the type of DDR SDRAM device used. This selection is necessary for the Address Calculation. The address is calculated based on Figure 2–1 on page 2–8.

14 X 11 (default)
14 X 10
13 X 11
13 X 10
13 X 9
12 X 10
12 X 9
12 X 8

CAS latency. Choose among the following selections depending on the CAS latency of the DDR SDRAM device.

1.5 (default)
2
2.5
3

Registered?. Choose among the following selections depending on whether the registered DDR memory is used.

No (default)
Yes

Prefetch byte ordering. Choose among the following selections depending on the byte ordering.

Big edian (default)
Little edian

Figure 2–1 shows address multiplexing for DDR-SDRAM memories.

ROW x COL		msb			Address from Core Master																											lsb
		0–3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33–35
14 x 11	RAS				13	12	11	10	9	8	7	6	5	4	3	2	1	0														
	MBA																		1	0												
	CAS																				11	9	8	7	6	5	4	3	2	1	0	
14 x 10	RAS					13	12	11	10	9	8	7	6	5	4	3	2	1	0													
	MBA																			1	0											
	CAS																					9	8	7	6	5	4	3	2	1	0	
13 x 11	RAS					12	11	10	9	8	7	6	5	4	3	2	1	0														
	MBA																		1	0												
	CAS																				11	9	8	7	6	5	4	3	2	1	0	
13 x 10	RAS						12	11	10	9	8	7	6	5	4	3	2	1	0													
	MBA																			1	0											
	CAS																					9	8	7	6	5	4	3	2	1	0	
13 x 9	RAS							12	11	10	9	8	7	6	5	4	3	2	1	0												
	MBA																				1	0										
	CAS																						8	7	6	5	4	3	2	1	0	
12 x 10	RAS							11	10	9	8	7	6	5	4	3	2	1	0													
	MBA																			1	0											
	CAS																					9	8	7	6	5	4	3	2	1	0	
12 x 9	RAS								11	10	9	8	7	6	5	4	3	2	1	0												
	MBA																				1	0										
	CAS																						8	7	6	5	4	3	2	1	0	
12 x 8	RAS									11	10	9	8	7	6	5	4	3	2	1	0											
	MBA																					1	0									
	CAS																							7	6	5	4	3	2	1	0	

Figure 2–1: Address Multiplexing for DDR–SDRAM memories.

Microprocessor Specific Fields for the 85XXDDR_RW Support Package

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways.

Show DESELECT cycles. Choose from the following selections depending on whether you want to see DESELECT cycles in the Listing Window.

Yes (Default)
No

Show all data?. Choose among the following selections depending on whether you want to see Valid Data in the Listing Window.

Yes (default)
No

Processor used. Choose between the following microprocessors.

MPC8540 (default)
MPC8560

Debug Signals. Choose among the following selections depending on where the debug signals are available.

Disabled
Debug signals on MSRCID
Debug signals on ECC

DDR configuration. Choose among the following selections depending on the type of DDR SDRAM device used. This selection is necessary for the Address Calculation. The address is calculated based on the figure 2–1 on page 2-8.

14 X 11 (default)
14 X 10
13 X 11
13 X 10
13 X 9
12 X 10
12 X 9
12 X 8

CAS Latency. Choose among the following selections depending on the CAS latency of the DDR SDRAM device.

1.5 (default)
2
2.5
3

Registered?. Choose among the following selections depending on whether registered DDR memory is used.

No (default)
Yes

Prefetch byte ordering. Choose among the following selections depending on the byte ordering.

Big endian (default)
Little endian

Microprocessor Specific Fields for the 85XXLB, 85XXLB_ALT, and 85XXLB_ADS Support Package

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways.

Show. Choose among the following selections depending on which cycles you wish to see in the Listing Window.

All cycles (default)
GPCM cycles
SDRAM cycles
UPM cycles

Debug Signals. Choose among the following selections depending on where the debug signals are available.

Disabled (default)
Enabled

LCS [0:7]-machine select. Enter an 8-digit number "xxxxxxxx" where each digit corresponds to the type of machine connected to CS0 to CS7. Select x as follows.

x=0 for GPCM
x=1 for SDRAM
x=2 for UPM
x=4 if no memory is connected

For example if LCS0, LCS1, and LCS2 have SDRAM; LCS3 and LCS4 have UPM; LCS5 and LCS6 have GPCM and no memory device is connected to LCS7 then the 8-digit number for this option is “11122004”

LCS [0:7]-port size select. Enter an 8-digit number “xxxxxxxx” where each digit corresponds to the port size of each machine connected to CS0 to CS7. Select x as follows.

x=0 for 32-bit
x=1 for 16-bit
x=2 for 8-bit
x=4 if no memory is connected

For example, if LCS0, LCS1, and LCS2 are connected to devices with port width of 32-bits, LCS3 and LCS4 are connected to devices with port width of 16-bits, LCS5 and LCS6 are connected to devices of port width of 8-bits and no memory device is connected to LCS7 then the 8-digit number for this option is “00011224”

SDRAM CAS latency. Choose among the following selections depending on the CAS latency of the local bus SDRAM device.

One (default)
Two
Three

Cycle Type Labels

The TMS568 MPC85XX microprocessor support product decodes and displays the cycle type labels in the hardware display format.

Table 2–2 lists the cycle type labels and their descriptions.

Table 2–2: Cycle type labels

Label	Description
Flush	This cycle is fetched but not executed.
Extension	This cycle is an extension to a preceding instruction opcode.
Unknown	This combination of control bits is unexpected or unrecognized.

Table 2–3 lists the computed cycle type labels and their descriptions.

Table 2–3: Computed cycle type labels

Label	Description
Read	Read cycle
Write	Write cycle
System Reset	Reset cycle
Refresh	Refresh cycle
Precharge	Bank precharge cycle
Precharge all	Precharge all bank cycle
Row Address	Row address
Column address	Column address

Interrupt and Exception Labels

The e500 core supports extended exception handling model, with nested interrupt capability and extensive interrupt vector programmability. There are many registers associated with Interrupt and Exception labels. Two are explained in detail here.

- IVPR (Interrupt vector prefix register): IVPR[32–47] contains the high-order 16 bits of the address of the exception processing routines defined in the IVOR registers.
- IVOR (Interrupt vector offset register): The IVORs contain the low-order offset of the address of the exception processing routines defined in the IVOR registers.

Each interrupt has an associated interrupt vector address, obtained by computing the IVPR value with the address index in the associated IVOR (that is, IVPR[32–47]||IVORn[48–59]||0b0000). The resulting address is that of the instruction to be executed when that interrupt occurs. IVPR and IVOR values are indeterminate on reset.

For example, you can store the interrupt routine in any memory location, specifying the interrupt prefix and offset values in the registers.

The TMS568 MPC85XX microprocessor software product labels all exception vector reads, using the following symbols in address column: (See the MPC85XX Microprocessor User Manual for the description of these labels).

Critical_input_interrupt
Data_storage_interrupt
Instruction_storage_interrupt

External_input_interrupt
Alignment_interrupt
Program_interrupt
Floating-point_unavailable_interrupt
System_call_interrupt
Auxiliary_processor_unavailable_interrupt
Decrementer_interrupt
Fixed-interval_interrupt
Watchdog_timer_interrupt
Data_TLB_error_interrupt
Instruction_TLB_error_interrupt
Debug_interrupt
SPE_APU_unavailable_interrupt
SPE_floating-point_data_exception
SPE_floating-point_round_exception
Performance_monitor

These labels are defined in the DemoAddr.tsf in each support folder. You can edit this file for the interrupt table. Each label provides a vector address. For example, IVPR[32-47]||IVORn[48-59]||0b0000).

Special Characters

This section gives information about the special messages used in the TMS568 MPC85XX microprocessor support product. The disassembler uses special messages to indicate the following significant events.

Table 2-4 lists the special messages and their descriptions.

Table 2-4: Special messages and their descriptions

Special messages	Description
#	This indicates the current value depending on the target microprocessor's assembler notation.
>	This indicates that there is insufficient room on the screen to show all the available data.
>>	This indicates that the instruction fetch cycle has been manually marked.
t	This indicates that the given number is in decimal. For example: #12t (for 0xC in hexadecimal).
****	This string indicates that there is insufficient data available for complete disassembly of the instruction. The number of asterisks indicates the "width" of the data that is unavailable. Two asterisks represent a byte.

Viewing Disassembled Data

You can view disassembled data for the TMS568 MPC85XX microprocessor support product in four display formats:

Hardware
Software
Control Flow
Subroutine

All disassembly modes are available through the “Disassembly Properties” menu of the listing display.

The information on basic operations describes how to select the disassembly display formats.

If a channel group is not visible, you must use Add Column or Ctrl+L to make the group visible.

Hardware Display Format

In the hardware display format, all valid opcode fetch bus cycles is disassembled and displayed. Noninstruction bus cycles are displayed with the appropriate cycle type labels. This is the default format for disassembly.

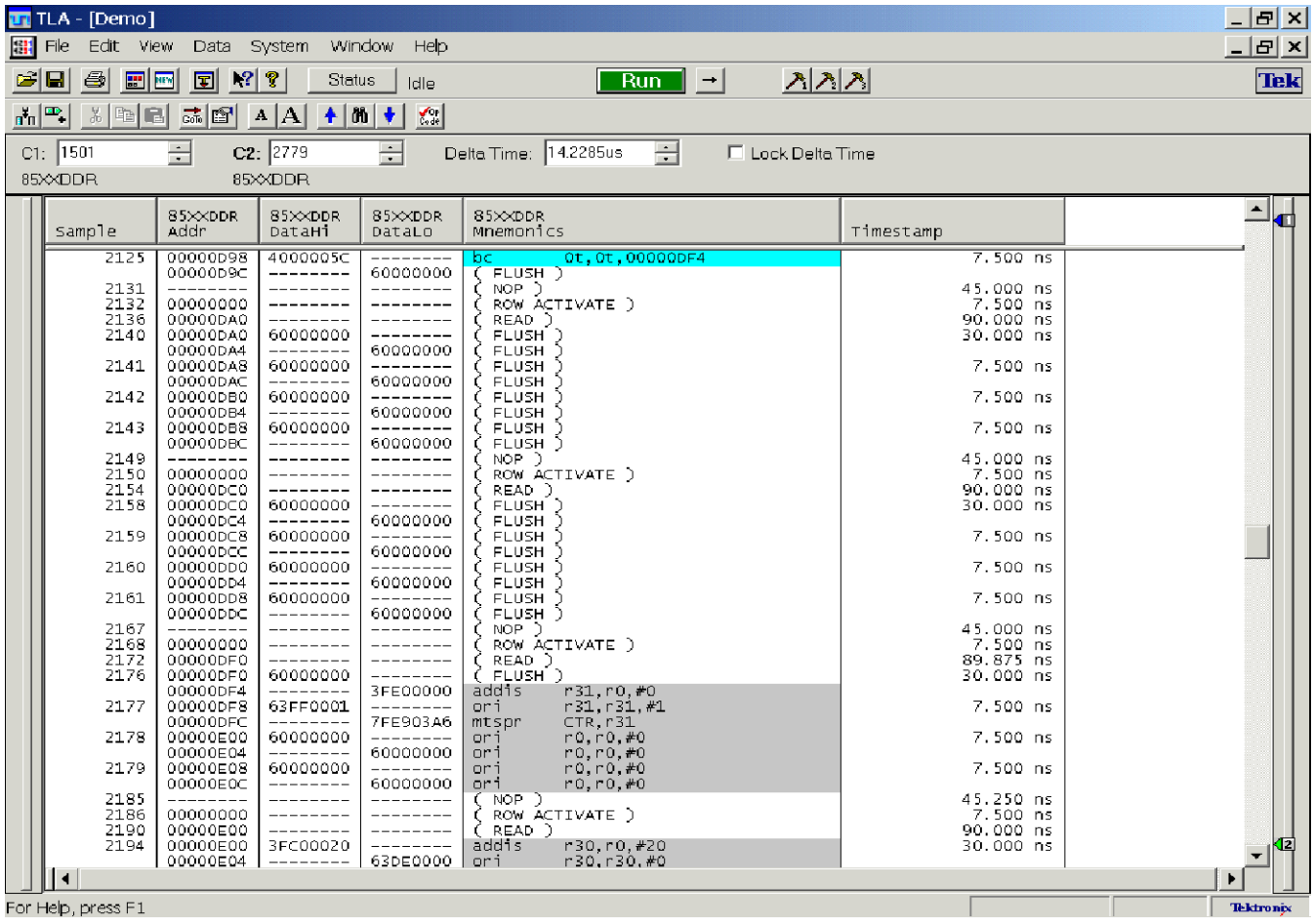


Figure 2-2: 85XXDDR hardware display format

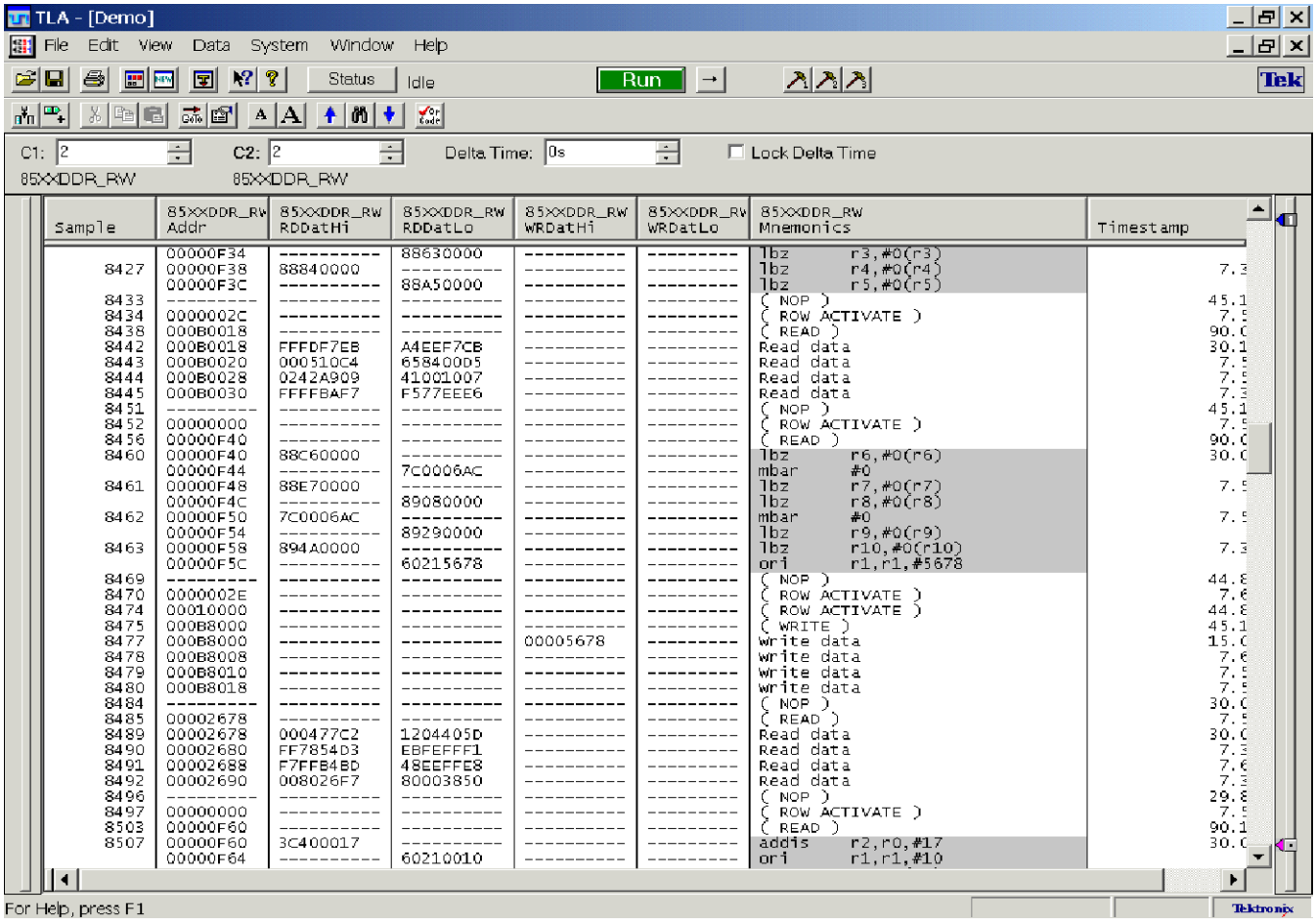


Figure 2-3: 85XXDDR_RW hardware display format

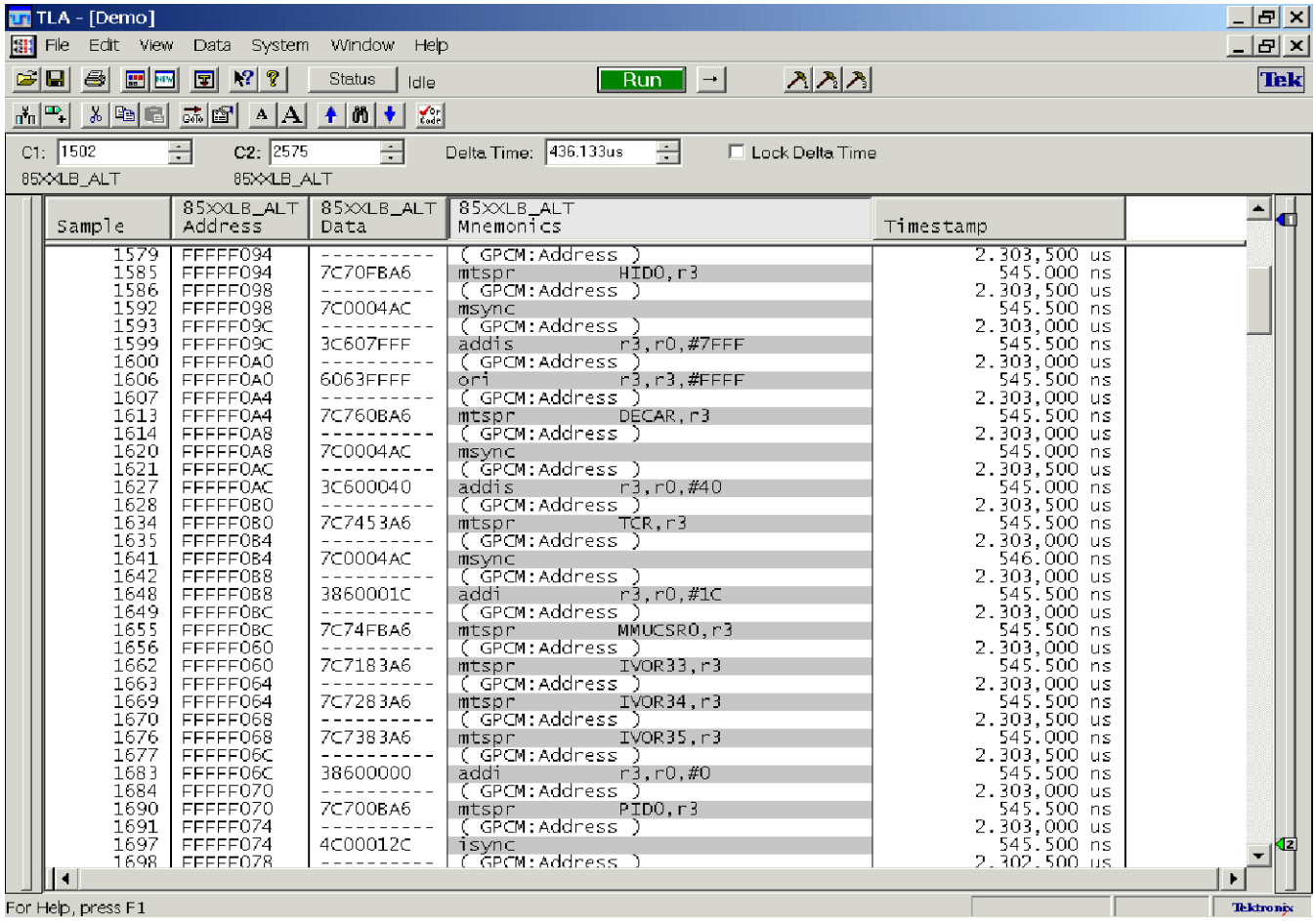


Figure 2-4: 85XXLB_ALT hardware display format

Software Display Format

In the software display format only the first opcode fetch of executed instruction cycles is displayed (read extensions are used to disassemble the instruction but are not displayed as separate cycles in software mode). Noninstruction bus cycles are not displayed in software mode. Any “special” cycles that are described as showing up in Control Flow or Subroutine display formats are displayed here.

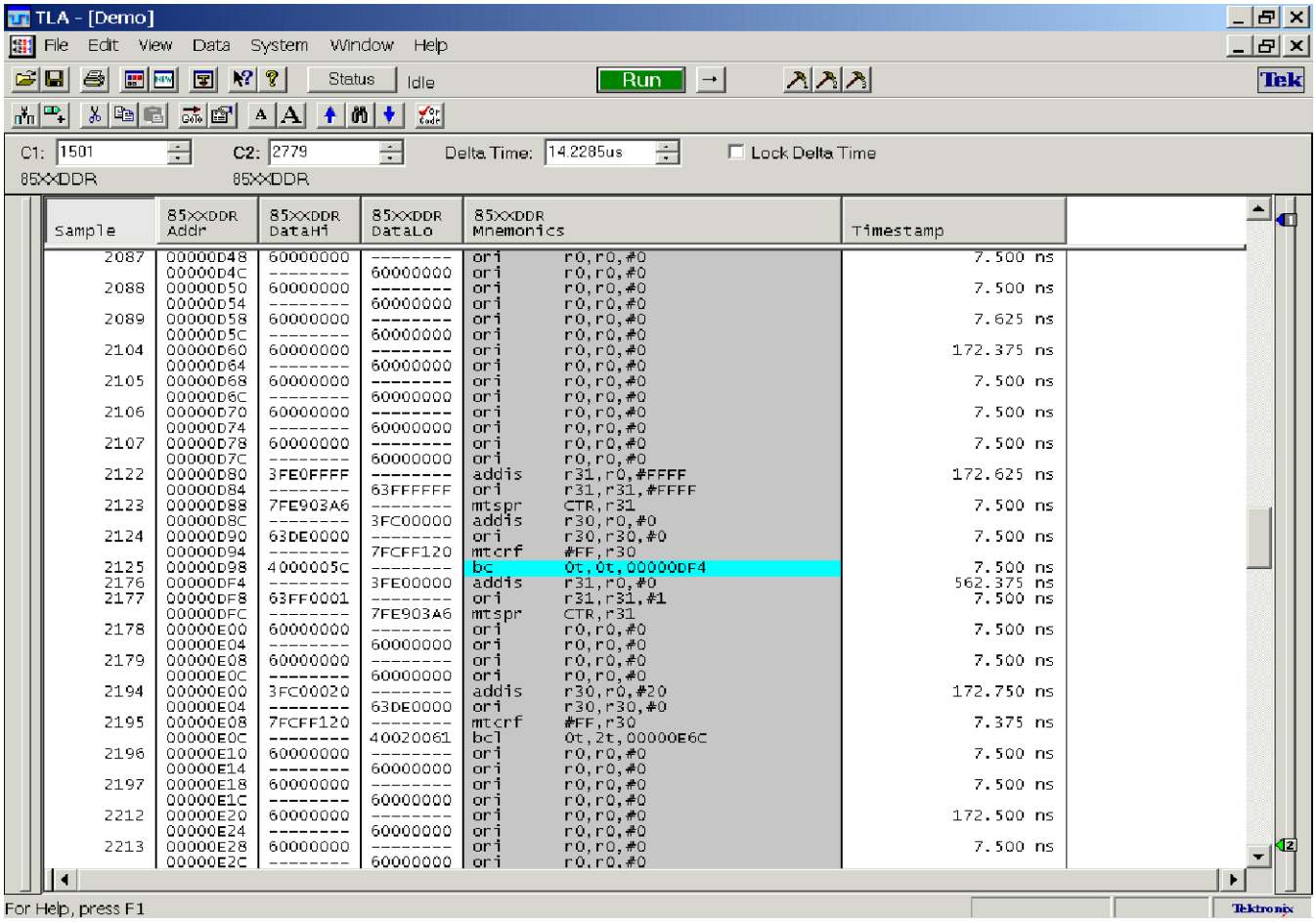


Figure 2-5: 85XXDDR software display format

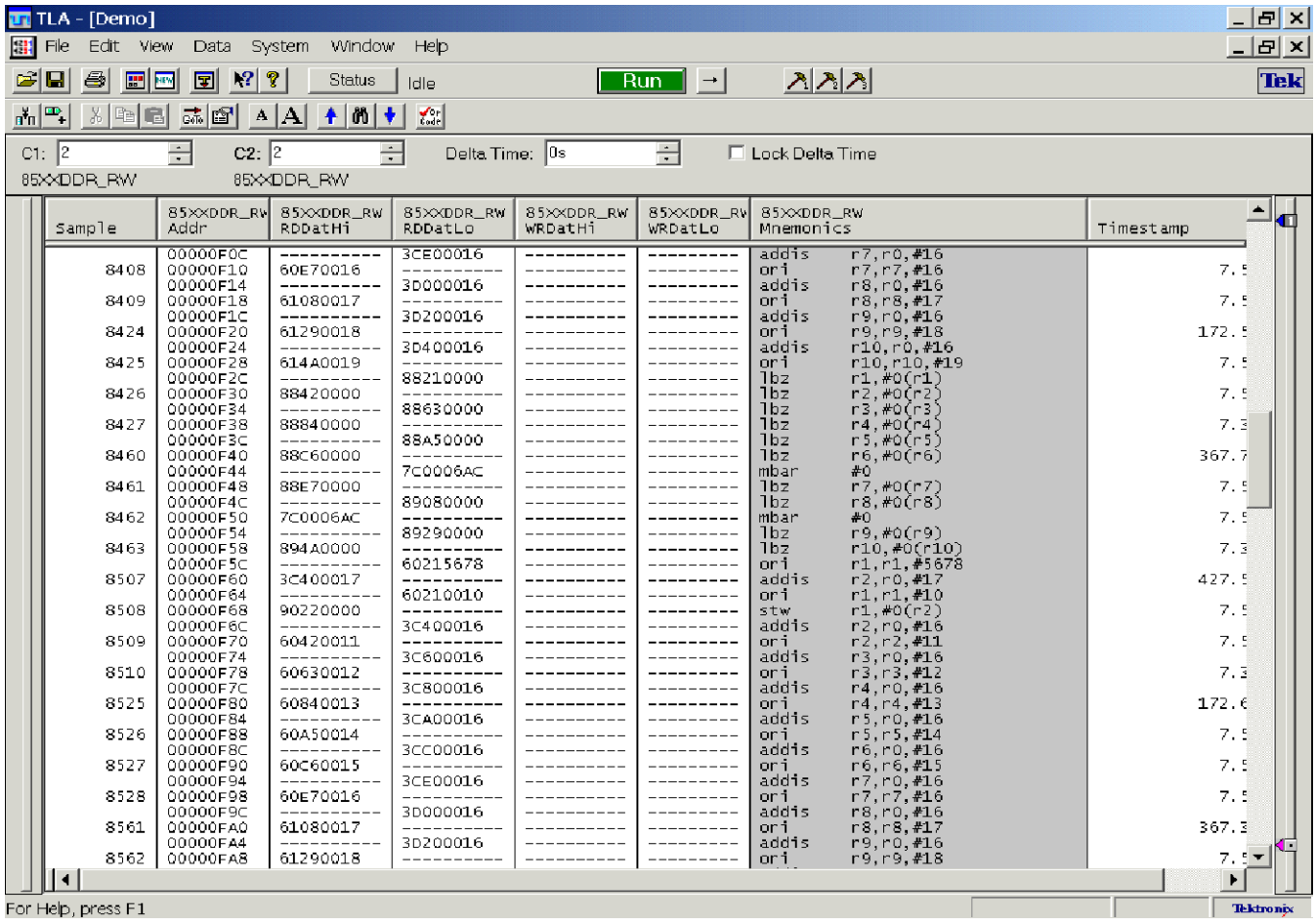


Figure 2-6: 85XXDDR_RW software display format

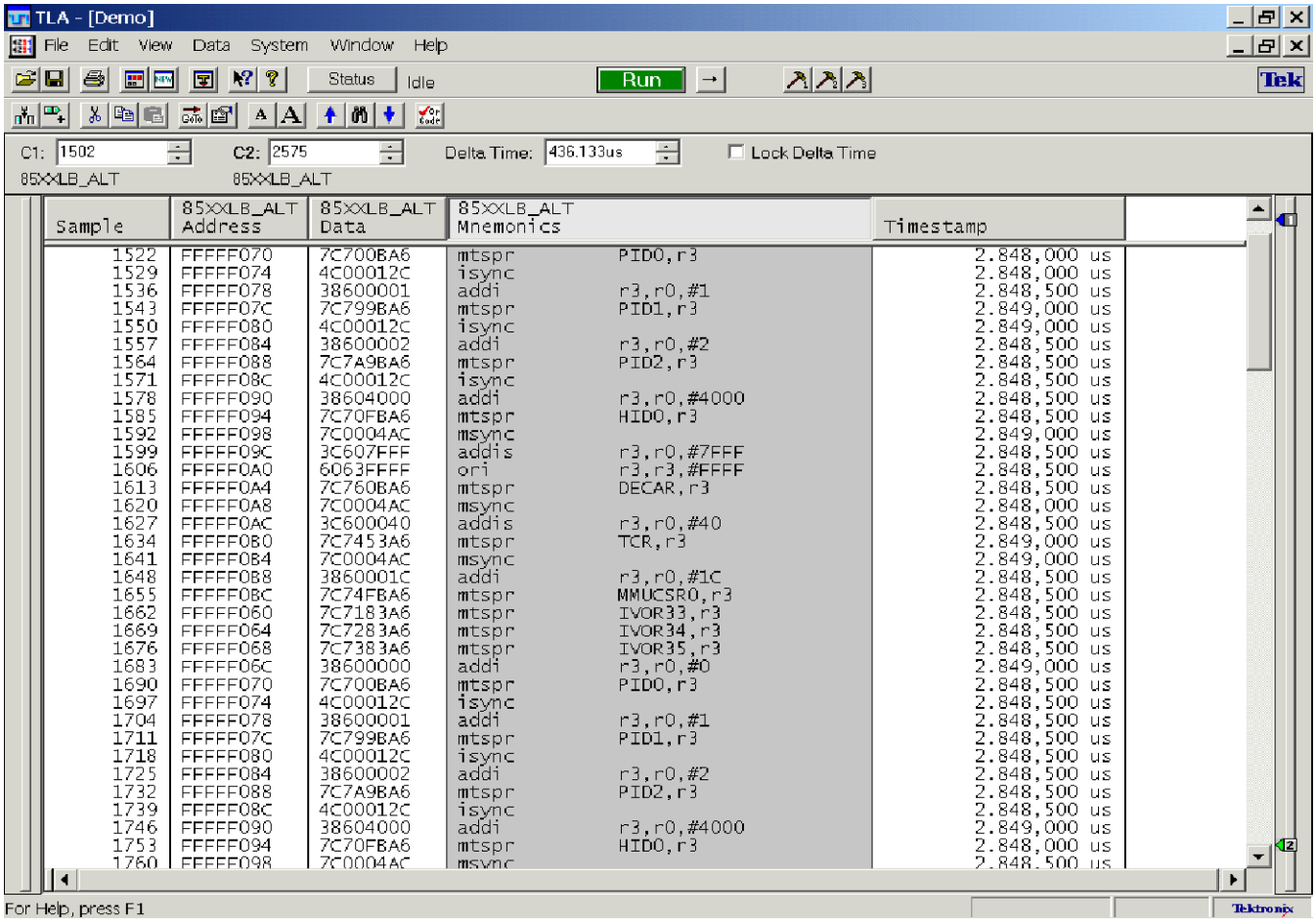


Figure 2-7: 85XXLB_ALT software display format

Control Flow Display Format

In Control Flow display format, only the first opcode fetch of instructions that cause a branch in the addressing is displayed.

b target address	ba target address
bl target address	bla target address
sc	rfi

The following MPC85XX microprocessor instructions conditionally affect control flow and are displayed if they are taken.

bc BO, BI, target address	bca BO, BI, target address
bcl BO, BI, target address	bcla BO, BI, target address
bclr BO, BI	bclrl BO, BI
bcctr BO, BI	bcctrl BO, BI

The following MPC85XX microprocessor instructions are displayed if they cause an exception to happen (resulting in a change in the control flow).

tw twi
sc rfi

Any “special” cycles that are displayed in Subroutine display format are also displayed here.

Subroutine Display Format

In Subroutine display format, only the first opcode fetch of subroutine call and return instructions are displayed.

The following MPC85XX microprocessor instructions unconditionally affect subroutine display:

tw twi isync

The following MPC85XX microprocessor instructions are displayed if they cause an exception:

sc rfi

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Use this function to select a cycle and change it.

Marks are placed by using the Mark Opcode button. The Mark Opcode button is always available. When a cycle is marked, the character “>>” is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the “Undo Mark” selection, which removes the character “>>”.

If the sample being marked is an Address or SDRAM command cycle, Mark Opcode selections are replaced by a note indicating that “An Opcode Mark cannot be placed at the selected data sample”.

Table 2-5 lists Mark selections and definitions for 85XXLB and 85XXLB_ALT and 85XXLB_ADS support packages.

Table 2-5: Mark selections and definitions in 85XXLB, 85XXLB_ALT, and 85XXLB_ADS

Mark selection or combination	Definition
Read->Fetch	Fetch cycle is marked as read cycle
Undo Mark	Removes all marks from the current sequence

Table 2–6 lists Mark selections and definitions for 85XXDDR and 85XXDDR_RW support packages.

Table 2–6: Mark selections and definitions in 85XXDDR and 85XXDDR_RW

Mark selection or combination	Definition
Opcode – Opcode	DataHi or RDDatHi and DataLo or RDDatLo are disassembled
Opcode – Flush	Only DataHi or RDDatHi is disassembled in Big Endian mode and DataLo or RDDatLo is disassembled in Little Endian mode
Flush – Opcode	Only DataHi or RDDatHi is disassembled in Little Endian mode and DataLo or RDDatLo is disassembled in Big Endian mode
Flush – Flush	Instructions not disassembled and labeled as (Flush)
Read -> Fetch	Read is marked as a Fetch and disassembled
Undo Mark	Removes all marks from the current sequence

***NOTE**. DataHi and DataLo corresponds to 85XXDDR support package. RDDatHi and RDDatLo corresponds to 85XXDDR_RW support package.*

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided on your disk for the three support packages 85XXLB_ALT, 85XXDDR, and 85XXDDR_RW so you can see an example of how your TMS568 MPC85XX microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the file system is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your target system.

Information on basic operations describes how to view the file.

Reference

Channel Group Definitions

This section lists the channel group definitions required for disassembly, for the TMS568 MPC85XX microprocessor support product.

Channel Groups

The software automatically defines channel groups for the support package. Tables 3–1 through 3–3 show the channel groups for the TMS568 MPC85XX microprocessor support product for the 85XXDDR, 85XXDDR_RW, 85XXLB, 85XXLB_ALT, and 85XXLB_ADS support packages.

Table 3–1: 85XXDDR support package channel groups

Group name	Display radix
Address	Hexadecimal
BankAddr	Off
DataLo	Hexadecimal
DataHi	Hexadecimal
Mnemonics	Dissasembly generated text
Control	Off
Command	Off
Strobes	Off
ChipSel	Off
CheckBits	Off
WrtMasks	Off
Debug	Off
Misc	Off
UserDefined	Off
DatByte0	Off
DatByte1	Off
DatByte2	Off
DatByte3	Off
DatByte4	Off
DatByte5	Off
DatByte6	Off

Table 3-1: 85XXDDR support package channel groups (Cont.)

Group name	Display radix
DatByte7	Off
Timestamp	

Table 3-2: 85XXDDR_RW support package channel groups

Group name	Display radix
Address	Hexadecimal
BankAddr	Off
RdDatLo	Hexadecimal
RdDatHi	Hexadecimal
WrDatLo	Hexadecimal
WrDatHi	Hexadecimal
Mnemonics	Dissasembly generated text
Control	Off
Command	Off
Strobes	Off
ChipSel	Off
CheckBits	Off
WrtMasks	Off
Debug	Off
Misc	Off
UserDefined	Off
RDDatBy0	Off
RDDatBy1	Off
RDDatBy2	Off
RDDatBy3	Off
RDDatBy4	Off
RDDatBy5	Off
RDDatBy6	Off
RDDatBy7	Off
WRDatBy0	Off
WRDatBy1	Off
WRDatBy2	Off
WRDatBy3	Off

Table 3-2: 85XXDDR_RW support package channel groups (Cont.)

Group name	Display radix
WRDatBy4	Off
WRDatBy5	Off
WRDatBy6	Off
WRDatBy7	Off
Timestamp	

Table 3-3: 85XXLB, 85XXLB_ALT, 85XXLB_ADS support package channel groups

Group name	Display radix
Address	Hexadecimal
BurstAddr	Off
Data	Hexadecimal
Mnemonics	Dissasembly generated text
Control	Off
ChipSel	Off
Debug	Off
DataMask	Off
UserDefined	Off
Timestamp	

Symbol and Channel Assignment Tables

This section lists the symbol tables, channel assignment tables for disassembly and timing for each of the support packages.

Symbol Tables

The TMS568 MPC85XX microprocessor support product supplies three symbol table files each for the 85XXLB, 85XXLB_ALT, and 85XXLB_ADS support packages and two symbol tables each for 85XXDDR and 85XXDDR_RW support packages.

Tables 3–4 through 3–7 show the definitions for the symbol, bit pattern, and meaning of the group symbols in the control symbol tables.

Table 3- 4: 85XXLB, 85XXLB_ALT, 85XXLB_ADS ChipSel group symbol table definitions

Symbol	ChipSel group value LCS0~ LCS1~ LCS2~ LCS3~ LCS4~ LCS5~ LCS6~ LCS7~	Description
LCS0~	0 1 1 1 1 1 1 1	Chip Select 0
LCS1~	1 0 1 1 1 1 1 1	Chip Select 1
LCS2~	1 1 0 1 1 1 1 1	Chip Select 2
LCS3~	1 1 1 0 1 1 1 1	Chip Select 3
LCS4~	1 1 1 1 0 1 1 1	Chip Select 4
LCS5~	1 1 1 1 1 0 1 1	Chip Select 5
LCS6~	1 1 1 1 1 1 0 1	Chip Select 6
LCS7~	1 1 1 1 1 1 1 0	Chip Select 7

Table 3-5: 85XXLB, 85XXLB_ALT, 85XXLB_ADS Control group symbol table definitions

Symbol	Control group value				Description
	MDVAL	LSDDQM0/LWE0~ LSDDQM1/LWE1~ LSDDQM2/LWE2~ LSDDQM3/LWE3~	LGTA~ LBCTL LSDA10/LGPL0	LALE LSDRAS~/LBOE~ LSDCAS~/LGPL3 LSDWE~/LGPL1	
Address	X	XXXX	XXX	1XXX	Address cycle
SDRAM:Read	X	XXXX	XXX	X101	SDRAM Read cycle
SDRAM:Write	X	XXXX	XXX	X100	SDRAM Write cycle
SDRAM:Act/ GPCM:Read	X	XXXX	XXX	X011	SDRAM Activate/ GPCM Read cycle
SDRAM:Precharge	X	XXXX	XX0	X010	SDRAM Precharge cycle
SDRAM:Precharge-all	X	XXXX	XX1	X010	SDRAM Activate/ GPCM
SDRAM:Auto-Refresh	X	XXXX	XXX	X001	SDRAM Precharge cycle
SDRAM:Mode-Set	X	XXXX	XXX	X000	SDRAM Precharge-all cycle
GPCM:LGTA~	X	XXXX	0XX	XXXX	SDRAM Auto-Refresh cycle
Write	X	XXX0	XXX	X1XX	GPCM Transfer Termination
Write	X	XX0X	XXX	X1XX	GPCM or SDRAM write cycle
Write	X	X0XX	XXX	X1XX	GPCM or SDRAM write cycle
Write	X	0XXX	XXX	X1XX	GPCM or SDRAM write cycle
DataValid	1	XXXX	XXX	XXXX	Local Bus Data Valid

Table 3-6: 85XXLB, 85XXLB_ALT, 85XXLB_ADS, 85XXDDR, and 85XXDDR_RW Debug group symbol table definitions

Symbol	Debug group value MDVAL MSRCID1 MSRCID0 MSRCID2 MSRCID3 MSRCID4
PCI	1 0 0 0 0 0
Reserved	1 0 0 0 0 1
Reserved	1 0 0 0 1 0
Reserved	1 0 0 0 1 1
Local Bus	1 0 0 1 0 0
Reserved	1 0 0 1 0 1
Reserved	1 0 0 1 1 0
Reserved	1 0 0 1 1 1
Configuration	1 0 1 0 0 0
Reserved	1 0 1 0 0 1
Boot Sequence	1 0 1 0 1 0
Reserved	1 0 1 0 1 1
Rapid_IO	1 0 1 1 0 0
Reserved	1 0 1 1 0 1
Reserved	1 0 1 1 1 0
Local_Space (DDR)	1 0 1 1 1 1
INSTR_Fetch	1 1 0 0 0 0
Data_Fetch	1 1 0 0 0 1
Reserved	1 1 0 0 1 0
Reserved	1 1 0 0 1 1
CPM	1 1 0 1 0 0
DMA	1 1 0 1 0 1
Reserved	1 1 0 1 1 0
SAP	1 1 0 1 1 1
Ethernet_0	1 1 1 0 0 0
Ethernet_1	1 1 1 0 0 1
Ethernet_2	1 1 1 0 1 0
Reserved	1 1 1 0 1 1
Rapid_IO_Msg	1 1 1 1 0 0
Rapid_IO_Doorbell	1 1 1 1 0 1
Rapid_IO_Port_Write	1 1 1 1 1 0
InValid Port	1 1 1 1 1 1

Table 3-7: 85XXDDR AND 85XXDDR_RW Control group symbol table definitions

Symbol	Control group value RESET~ MDVAL CS1~ CS0~ MRAS~ MCAS~ MWE~
DESL-IGNORE_COMMAND--DATA?	X X 1 1 X X X
NOP-NO OPERATION (S0~)	X X X 0 1 1 1
NOP-NO OPERATION (S1~)	X X 0 X 1 1 1
BST-BURST STOP (S0~)	X X X 0 1 1 0
BST-BURST STOP (S1~)	X X 0 X 1 1 0
READ-COL ADDR_READ_(S0~)	X X X 0 1 0 1
READ-COL_ADDR_READ_(S1~)	X X 0 X 1 0 1
WRITE-COL_ADDR_WRITE_(S0~)	X X X 0 1 0 0
WRITE-COL_ADDR_WRITE_(S1~)	X X 0 X 1 0 0
ACTV-ROW_ADDRESS_STROBE_(S0~)	X X X 0 0 1 1
PRE-PRECHARGE_SELECT_BANK_(S0~)	X X X 0 0 1 0
PRE-PRECHARGE_SELECT_BANK_(S1~)	X X 0 X 0 1 0
PALL-PRECHARGE_(S0~)	X X X 0 0 1 0
PALL-PRECHARGE_(S1~)	X X 0 X 0 1 0
REF-REFRESH_(S0~)	X X X 0 0 0 1
REF-REFRESH_(S1~)	X X 0 X 0 0 1
MRS-MODE_REGISTER_SET_(S0~)	X X X 0 0 0 0
MRS-MODE_REG_SET_(S1~)	X X 0 X 0 0 0

Channel Assignment Tables

Channel assignments shown in tables 3–8 through 3–66 use the following conventions:

- All signals are required by the support package, unless indicated otherwise.
- Channels are shown starting with the most significant bit, descending to the least significant bit.
- Channel group assignments are for all modules, unless otherwise noted.

85XXDDR Channel Group Assignments

Tables 3–8 through 3–28 show the channel assignments for the logic analyzer groups for the 85XXDDR support package and the microprocessor signal to which each channel connects.

Table 3–8 lists the channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-8: Address group assignments for 85XXDDR support package

Bit order	Section:Channel	85XXDDR support package channel name
14 (MSB)	C3:2	MA14
13	C3:7	MA13
12	D1:4	MA12
11	D2:1	MA11
10	E2:0	MA10
9	A2:1	MA9
8	A2:4	MA8
7	D2:3	MA7
6	D3:0	MA6
5	D2:6	MA5
4	D3:1	MA4
3	D3:2	MA3
2	A3:3	MA2
1	A3:5	MA1
0 (LSB)	E0:0	MA0

Table 3–9 lists the channel assignments for the BankAddr group and the microprocessor signal to which each channel connects. By default, this channel group is not displayed.

Table 3-9: BankAddr group assignments for 85XXDDR support package

Bit order	Section:Channel	85XXDDR support package channel name
2 (MSB)	E2:7	MBA0
1	E0:3	MBA1
0 (LSB)	D1:7	MBA2

Table 3–10 lists the channel assignments for the DataLo group and the microprocessor signal to which each channel connects. By default, this group is displayed in hexadecimal.

Table 3-10: DataLo group assignments for 85XXDDR support package

Bit order	Section:Channel	85XXDDR support package channel name
31 (MSB)	D0:0	MDQ0
30	D0:1	MDQ1
29	A0:2	MDQ2
28	D0:4	MDQ3
27	A0:0	MDQ4
26	A0:1	MDQ5
25	A0:4	MDQ6
24	A0:3	MDQ7
23	A0:7	MDQ8
22	D0:7	MDQ9
21	A1:1	MDQ10
20	D1:2	MDQ11
19	A1:2	MDQ12
18	A1:6	MDQ13
17	A1:5	MDQ14
16	A1:4	MDQ15
15	D1:1	MDQ16
14	D1:5	MDQ17
13	D2:4	MDQ18
12	D2:5	MDQ19
11	D1:3	MDQ20
10	A2:0	MDQ21
9	A2:2	MDQ22
8	A2:3	MDQ23
7	A2:5	MDQ24
6	D2:7	MDQ25
5	A3:2	MDQ26
4	A3:4	MDQ27
3	A2:6	MDQ28

Table 3-10: DataLo group assignments for 85XXDDR support package (Cont.)

Bit order	Section:Channel	85XXDDR support package channel name
2	A3:0	MDQ29
1	D3:4	MDQ30
0 (LSB)	D3:3	MDQ31

Table 3–11 lists the channel assignments for the DataHi group and the microprocessor signal to which each channel connects. By default, this group is displayed in hexadecimal.

Table 3-11: DataHi group assignments for 85XXDDR support package

Bit order	Section:Channel	85XXDDR support package channel name
31 (MSB)	E2:4	MDQ32
30	E0:5	MDQ33
29	E2:6	MDQ34
28	E3:1	MDQ35
27	E2:3	MDQ36
26	E2:5	MDQ37
25	E0:7	MDQ38
24	E3:0	MDQ39
23	E3:2	MDQ40
22	E3:3	MDQ41
21	E1:3	MDQ42
20	E1:6	MDQ43
19	E3:4	MDQ44
18	E3:6	MDQ45
17	E1:7	MDQ46
16	E1:2	MDQ47
15	E1:5	MDQ48
14	C0:0	MDQ49
13	C0:5	MDQ50
12	C3:4	MDQ51
11	C0:1	MDQ52

Table 3-11: DataHi group assignments for 85XXDDR support package (Cont.)

Bit order	Section:Channel	85XXDDR support package channel name
10	C0:2	MDQ53
9	C3:3	MDQ54
8	C0:3	MDQ55
7	C2:7	MDQ56
6	C3:0	MDQ57
5	C1:1	MDQ58
4	C1:2	MDQ59
3	C1:0	MDQ60
2	C3:1	MDQ61
1	C2:5	MDQ62
0 (LSB)	C2:4	MDQ63

Table 3–12 lists the channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-12: Control group assignments for 85XXDDR support package

Bit order	Section:Channel	85XXDDR support package channel name
6 (MSB)	A0:6	RESET~
5	Qual:0	MDVAL
4	C2:0	MCS1~
3	C2:3	MCS0~
2	C2:2	MRAS~
1	C2:1	MCAS~
0 (LSB)	Qual:3	MWE~

Table 3–13 lists the channel assignments for the command group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-13: Command group assignments for 85XXDDR support packages

Bit order	Section:Channel	85XXDDR support package channel name
4 (MSB)	C2:0	MCS1~
3	C2:3	MCS0~
2	C2:2	MRAS~
1	C2:1	MCAS~
0 (LSB)	Qual:3	MWE~

Table 3–14 lists the channel assignments for the Strobes group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-14: Strobes group assignments for 85XXDDR support package

Bit order	Section:Channel	85XXDDR support package channel name
7 (MSB)	D0:2	MDQS0
6	A1:3	MDQS1
5	D2:0	MDQS2
4	A2:7	MDQS3
3	E0:6	MDQS4
2	E3:5	MDQS5
1	C3:5	MDQS6
0 (LSB)	C2:6	MDQS7

Table 3–15 lists the channel assignments for the ChipSel group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-15: ChipSel group assignments for 85XXDDR support package

Bit order	Section:Channel	85XXDDR support package channel name
3 (MSB)	C2:3	MCS0~
2	C2:0	MCS1~
1	E1:1	MCS2~
0 (LSB)	E1:4	MCS3~

Table 3–16 lists the channel assignments for the CheckBits group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-16: CheckBits group assignments for 85XXDDR support package

Bit order	Section:Channel	85XXDDR support package channel name
7	D3:6	ECC0
6	A3:7	ECC1
5	E0:2	ECC2
4	E2:1	ECC3
3	D3:5	ECC4
2	A3:6	ECC5
1	E0:4	ECC6
0	E2:2	ECC7

Table 3–17 lists the channel assignments for the WrtMasks group assignments for the 85XXDDR support package. By default, this group is not displayed.

Table 3-17: WrtMasks group assignments for 85XXDDR support package

Bit order	Section:Channel	85XXDDR support package channel name
7 (MSB)	D0:3	MDM0
6	A1:7	MDM1

Table 3-17: WrtMasks group assignments for 85XXDDR support package (Cont.)

Bit order	Section:Channel	85XXDDR support package channel name
5	D2:2	MDM2
4	A3:1	MDM3
3	E1:0	MDM4
2	E3:7	MDM5
1	C3:6	MDM6
0 (LSB)	C0:7	MDM7

Table 3–18 lists the channel assignments for the Debug group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-18: Debug group assignments for the 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
4 (MSB)	A0:5	MSRCID0
3	Clock:2	MSRCID1
2	D1:0	MSRCID2
1	D0:6	MSRCID3
0 (LSB)	D0:5	MSRCID4

Table 3–19 lists the channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-19: Misc group assignments for 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
2 (MSB)	Clock:0	MCK0
1	Clock:1	MCK1
0 (LSB)	Clock:3	MCK2

Table 3–20 lists the channel assignments for the UserDefined group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-20: UserDefined group assignments for the 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
12 (MSB)	Qual:2	NC–No signal
11	Qual:1	SCL
10	D1:6	MCKE0
9	A1:0	MCKE1
8	C1:4	SA0
7	C1:6	SA1
6	C1:5	SA2
5	C1:7	SDA
4	C0:6	VDDID
3	C1:3	TRIG_IN
2	C0:4	TRIG_OUT
1	E0:1	DM8
0 (LSB)	D3:7	DQS8

Table 3–21 lists the channel assignments for the DatByte0 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-21: DatByte0 group assignments for 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
8 (MSB)	D0:3	MDM0
7	D0:0	MDQ0
6	D0:1	MDQ1
5	A0:2	MDQ2
4	D0:4	MDQ3
3	A0:0	MDQ4
2	A0:1	MDQ5

Table 3-21: DatByte0 group assignments for 85XXDDR support package (Cont.)

Bit order	Section: Channel	85XXDDR support package channel name
1	A0:4	MDQ6
0 (LSB)	A0:3	MDQ7

Table 3–22 lists the channel assignments for the DatByte1 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-22: DatByte1 group assignments for 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
8 (MSB)	A1:7	MDM1
7	A0:7	MDQ8
6	D0:7	MDQ9
5	A1:1	MDQ10
4	D1:2	MDQ11
3	A1:2	MDQ12
2	A1:6	MDQ13
1	A1:5	MDQ14
0 (LSB)	A1:4	MDQ15

Table 3–23 lists the channel assignments for the DatByte2 user defined group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-23: DatByte2 group assignments for 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
8 (MSB)	D2:2	MDM2
7	D1:1	MDQ16
6	D1:5	MDQ17
5	D2:4	MDQ18
4	D2:5	MDQ19
3	D1:3	MDQ20

Table 3-23: DatByte2 group assignments for 85XXDDR support package (Cont.)

Bit order	Section: Channel	85XXDDR support package channel name
2	A2:0	MDQ21
1	A2:2	MDQ22
0 (LSB)	A2:3	MDQ23

Table 3–24 lists the channel assignments for the DatByte3 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-24: DatByte3 group assignments for 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
8	A3:1	MDM3
7	A2:5	MDQ24
6	D2:7	MDQ25
5	A3:2	MDQ26
4	A3:4	MDQ27
3	A2:6	MDQ28
2	A3:0	MDQ29
1	D3:4	MDQ30
0	D3:3	MDQ31

Table 3–25 lists the channel assignments for the DatByte4 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-25: DatByte4 group assignments for 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
8 (MSB)	E1:0	MDM4
7	E2:4	MDQ32
6	E0:5	MDQ33
5	E2:6	MDQ34
4	E3:1	MDQ35

Table 3-25: DatByte4 group assignments for 85XXDDR support package (Cont.)

Bit order	Section: Channel	85XXDDR support package channel name
3	E2:3	MDQ36
2	E2:5	MDQ37
1	E0:7	MDQ38
0 (LSB)	E3:0	MDQ39

Table 3–26 lists the channel assignments for the DatByte5 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-26: DatByte5 group assignments for 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
8 (MSB)	E3:7	MDM5
7	E3:2	MDQ40
6	E3:3	MDQ41
5	E1:3	MDQ42
4	E1:6	MDQ43
3	E3:4	MDQ44
2	E3:6	MDQ45
1	E1:7	MDQ46
0 (LSB)	E1:2	MDQ47

Table 3–27 lists the channel assignments for the DatByte6 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-27: DatByte6 group assignments for 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
8 (MSB)	C3:6	MDM6
7	E1:5	MDQ48
6	C0:0	MDQ49
5	C0:5	MDQ50

Table 3-27: DatByte6 group assignments for 85XXDDR support package (Cont.)

Bit order	Section: Channel	85XXDDR support package channel name
4	C3:4	MDQ51
3	C0:1	MDQ52
2	C0:2	MDQ53
1	C3:3	MDQ54
0 (LSB)	C0:3	MDQ55

Table 3–28 lists the channel assignments for the DatByte7 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-28: DatByte7 group assignments for 85XXDDR support package

Bit order	Section: Channel	85XXDDR support package channel name
8 (MSB)	C0:7	MDM7
7	C2:7	MDQ56
6	C3:0	MDQ57
5	C1:1	MDQ58
4	C1:2	MDQ59
3	C1:0	MDQ60
2	C3:1	MDQ61
1	C2:5	MDQ62
0 (LSB)	C2:4	MDQ63

85XXDDR_RW Channel Group Assignments

Tables 3–29 through 3–59 list the channel assignments for the logic analyzer groups for the 85XXDDR_RW support package.

Table 3–29 lists the Address group assignments for the 85XXDDR_RW support package. By default, this group is displayed in hexadecimal.

Table 3-29: Address group assignments for 85XXDDR_RW support package

Bit order	Section: Channel	85XXDDR_RW support package channel name
14 (MSB)	$0_C3:2	MA14
13	$0_C3:7	MA13
12	$1_E3:4	MA12
11	$1_C2:1	MA11
10	$0_E2:0	MA10
9	$0_A2:1	MA9
8	$0_A2:4	MA8
7	$1_C2:3	MA7
6	$1_C3:0	MA6
5	$1_C2:6	MA5
4	$1_C3:1	MA4
3	$1_C3:2	MA3
2	$0_A3:3	MA2
1	$0_A3:5	MA1
0 (LSB)	$1_A2:0	MA0

Table 3–30 lists the channel assignments for the BankAddr group and the microprocesser signal to which each channel connects. By default, this group is not displayed.

Table 3-30: BankAddr group assignments for 85XXDDR_RW support package

Bit order	Section: Channel	85XXDDR_RW support package channel name
2 (MSB)	$0_E2:7	MBA0
1	$1_A2:3	MBA1
0 (LSB)	$1_E3:7	MBA2

Table 3–31 lists the channel assignments for the RdDatLo group and the microprocesser signal to which each channel connects. By default, this group is displayed in hexadecimal.

Table 3-31: RdDatLo group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
31 (MSB)	$1_E2:0	MDQ0
30	$1_E2:1	MDQ1
29	$0_A0:2	MDQ2
28	$1_E2:4	MDQ3
27	$0_A0:0	MDQ4
26	$0_A0:1	MDQ5
25	$0_A0:4	MDQ6
24	$0_A0:3	MDQ7
23	$0_A0:7	MDQ8
22	$1_E2:7	MDQ9
21	$0_A1:1	MDQ10
20	$1_E3:2	MDQ11
19	$0_A1:2	MDQ12
18	$0_A1:6	MDQ13
17	$0_A1:5	MDQ14
16	$0_A1:4	MDQ15
15	$1_E3:1	MDQ16
14	$1_E3:5	MDQ17
13	$1_C2:4	MDQ18
12	$1_C2:5	MDQ19
11	$1_E3:3	MDQ20
10	$0_A2:0	MDQ21
9	$0_A2:2	MDQ22
8	$0_A2:3	MDQ23
7	$0_A2:5	MDQ24
6	$1_C2:7	MDQ25
5	$0_A3:2	MDQ26
4	$0_A3:4	MDQ27

Table 3-31: RdDatLo group assignments for 85XXDDR_RW support package (Cont.)

Bit order	Section:Channel	85XXDDR_RW support package channel name
3	$0_A2:6	MDQ28
2	$0_A3:0	MDQ29
1	$1_C3:4	MDQ30
0 (LSB)	$1_C3:3	MDQ31

Table 3–32 lists the channel assignments for the RdDatHi group and the microprocessor signal to which each channel connects. By default, this group is displayed in hexadecimal.

Table 3-32: RdDatHi group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
31(MSB)	$0_E2:4	MDQ32
30	$1_A2:5	MDQ33
29	$0_E2:6	MDQ34
28	$0_E3:1	MDQ35
27	$0_E2:3	MDQ36
26	$0_E2:5	MDQ37
25	$1_A2:7	MDQ38
24	$0_E3:0	MDQ39
23	$0_E3:2	MDQ40
22	$0_E3:3	MDQ41
21	$1_A3:3	MDQ42
20	$1_A3:6	MDQ43
19	$0_E3:4	MDQ44
18	$0_E3:6	MDQ45
17	$1_A3:7	MDQ46
16	$1_A3:2	MDQ47
15	$1_A3:5	MDQ48
14	$1_A0:0	MDQ49
13	$1_A0:5	MDQ50

Table 3-32: RdDatHi group assignments for 85XXDDR_RW support package (Cont.)

Bit order	Section:Channel	85XXDDR_RW support package channel name
12	$0_C3:4	MDQ51
11	$1_A0:1	MDQ52
10	$1_A0:2	MDQ53
9	$0_C3:3	MDQ54
8	$1_A0:3	MDQ55
7	$0_C2:7	MDQ56
6	$0_C3:0	MDQ57
5	$1_A1:1	MDQ58
4	$1_A1:2	MDQ59
3	$1_A1:0	MDQ60
2	$0_C3:1	MDQ61
1	$0_C2:5	MDQ62
0 (LSB)	$0_C2:4	MDQ63

Table 3–33 lists the channel assignments for the WrDatLo group and the microprocessor signal to which each channel connects. By default, this group is displayed in hexadecimal.

Table 3-33: WrDatLo group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
31 (MSB)	$1_E0:0	MDQ0_DM
30	$1_E0:1	MDQ1_DM
29	$0_D0:2	MDQ2_DM
28	$1_E0:4	MDQ3_DM
27	$0_D0:0	MDQ4_DM
26	$0_D0:1	MDQ5_DM
25	$0_D0:4	MDQ6_DM
24	$0_D0:3	MDQ7_DM
23	$0_D0:7	MDQ8_DM
22	$1_E0:7	MDQ9_DM

Table 3- 33: WrDatLo group assignments for 85XXDDR_RW support package (Cont.)

Bit order	Section:Channel	85XXDDR_RW support package channel name
21	$0_D1:1	MDQ10_DM
20	$1_E1:2	MDQ11_DM
19	$0_D1:2	MDQ12_DM
18	$0_D1:6	MDQ13_DM
17	$0_D1:5	MDQ14_DM
16	$0_D1:4	MDQ15_DM
15	$1_E1:1	MDQ16_DM
14	$1_E1:5	MDQ17_DM
13	$1_C0:4	MDQ18_DM
12	$1_C0:5	MDQ19_DM
11	$1_E1:3	MDQ20_DM
10	$0_D2:0	MDQ21_DM
9	$0_D2:2	MDQ22_DM
8	$0_D2:3	MDQ23_DM
7	$0_D2:5	MDQ24_DM
6	$1_C0:7	MDQ25_DM
5	$0_D3:2	MDQ26_DM
4	$0_D3:4	MDQ27_DM
3	$0_D2:6	MDQ28_DM
2	$0_D3:0	MDQ29_DM
1	$1_C1:4	MDQ30_DM
0 (LSB)	$1_C1:3	MDQ31_DM

Table 3–34 lists the channel assignments for the WrDatHi group and the microprocessor signal to which each channel connects. By default, this group is displayed in hexadecimal.

Table 3-34: WrDatHi group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
31 (MSB)	$0_E0:4	MDQ32_DM
30	$1_D2:5	MDQ33_DM
29	$0_E0:6	MDQ34_DM
28	$0_E1:1	MDQ35_DM
27	$0_E0:3	MDQ36_DM
26	$0_E0:5	MDQ37_DM
25	$1_D2:7	MDQ38_DM
24	$0_E1:0	MDQ39_DM
23	$0_E1:2	MDQ40_DM
22	$0_E1:3	MDQ41_DM
21	$1_D3:3	MDQ42_DM
20	$1_D3:6	MDQ43_DM
19	$0_E1:4	MDQ44_DM
18	$0_E1:6	MDQ45_DM
17	$1_D3:7	MDQ46_DM
16	$1_D3:2	MDQ47_DM
15	$1_D3:5	MDQ48_DM
14	$1_D0:0	MDQ49_DM
13	$1_D0:5	MDQ50_DM
12	$0_C1:4	MDQ51_DM
11	$1_D0:1	MDQ52_DM
10	$1_D0:2	MDQ53_DM
9	$0_C1:3	MDQ54_DM
8	$1_D0:3	MDQ55_DM
7	$0_C0:7	MDQ56_DM
6	$0_C1:0	MDQ57_DM
5	$1_D1:1	MDQ58_DM
4	$1_D1:2	MDQ59_DM

Table 3-34: WrDatHi group assignments for 85XXDDR_RW support package (Cont.)

Bit order	Section:Channel	85XXDDR_RW support package channel name
3	$1_D1:0	MDQ60_DM
2	$0_C1:1	MDQ61_DM
1	$0_C0:5	MDQ62_DM
0 (LSB)	$0_C0:4	MDQ63_DM

Table 3–35 lists the channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-35: Control group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
6 (MSB)	$0_A0:6	RESET~
5	$1_Clock:3	MDVAL
4	$0_C2:0	MCSI~
3	$0_C2:3	MCS0~
2	$0_C2:2	MRAS~
1	$0_C2:1	MCAS~
0 (LSB)	$0_Qual:3	MWE~

Table 3–36 lists the channel assignments for the Command group and the microprocessor signal to which each channel connects. By default, this group is displayed in symbols.

Table 3-36: Command group assignments for 85XXDDR_RW support package

Bit order	Section: Channel	85XXDDR_RW support package channel name
4 (MSB)	$0_C2:0	MCS1~
3	$0_C2:3	MCS0~
2	$0_C2:2	MRAS~

Table 3-36: Command group assignments for 85XXDDR_RW support package (Cont.)

Bit order	Section: Channel	85XXDDR_RW support package channel name
1	$0_C2:1	MCAS~
0 (LSB)	$0_Qual:3	MWE~

Table 3-37 lists the channel assignments for the Strobes group and the microprocessor signal to which each channel connects. By default, this group is displayed in symbols.

Table 3-37: Strobes group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7 (MSB)	$1_E2:2	MDQS0
6	$0_A1:3	MDQS1
5	$1_C2:0	MDQS2
4	$0_A2:7	MDQS3
3	$1_A2:6	MDQS4
2	$0_E3:5	MDQS5
1	$0_C3:5	MDQS6
0 (LSB)	$0_C2:6	MDQS7

Table 3-38 lists the channel assignments for the ChipSel group and the microprocessor signal to which each channel connects. By default, this group is displayed in symbols.

Table 3-38: ChipSel assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
3 (MSB)	$0_C2:3	MCS0~
2	$0_C2:0	MCS1~
1	$1_A3:1	MCS2~
0 (LSB)	$1_A3:4	MCS3~

Table 3–39 lists the channel assignments for the CheckBits group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-39: CheckBits group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7 (MSB)	$1_C3:6	ECC0
6	$0_A3:7	ECC1
5	$1_A2:2	ECC2
4	$0_E2:1	ECC3
3	$1_C3:5	ECC4
2	$0_A3:6	ECC5
1	$1_A2:4	ECC6
0 (LSB)	$0_E2:2	ECC7

Table 3–40 lists the channel assignments for the WrtMasks group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-40: WrtMasks group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7 (MSB)	$1_E2:3	MDM0
6	$0_A1:7	MDM1
5	$1_C2:2	MDM2
4	$0_A3:1	MDM3
3	$1_A3:0	MDM4
2	$0_E3:7	MDM5
1	$0_C3:6	MDM6
0 (LSB)	$1_A0:7	MDM7

Table 3–41 lists the channel assignments for the Debug group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-41: Debug group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
4 (MSB)	$0_A0:5	MSRCID0
3	$1_Qual:3	MSRCID1
2	$1_E3:0	MSRCID2
1	$1_E2:6	MSRCID3
0 (LSB)	$1_E2:5	MSRCID4

Table 3–42 lists the channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-42: Misc group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
2 (MSB)	$0_Clock:3	MCK2
1	$0_Clock:1	MCK1
0 (LSB)	$0_Clock:0	MCK0

Table 3–43 lists the channel assignments for the UserDefined group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-43: UserDefined group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
12 (MSB)	$1_Clock:0	NC–No signal
11	$1_Clock:1	SCL
10	$1_E3:6	MCKE0
9	$0_A1:0	MCKE1
8	$1_A1:4	SA0

Table 3-43: UserDefined group assignments for 85XXDDR_RW support package (Cont.)

Bit order	Section:Channel	85XXDDR_RW support package channel name
7	$1_A1:6	SA1
6	$1_A1:5	SA2
5	$1_A1:7	SDA
4	$1_A0:6	VDDID
3	$1_A1:3	TRIG_IN
2	$1_A0:4	TRIG_OUT
1	$1_A2:1	NC_DM8
0 (LSB)	$1_C3:7	NC_DQS8

Table 3–44 lists the channel assignments for the RDDatBy0 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-44: RDDatBy0 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7	$1_E2:0	MDQ0
6	$1_E2:1	MDQ1
5	$0_A0:2	MDQ2
4	$1_E2:4	MDQ3
3	$0_A0:0	MDQ4
2	$0_A0:1	MDQ5
1	$0_A0:4	MDQ6
0 (LSB)	$0_A0:3	MDQ7

Table 3–45 lists the channel assignments for the RDDatBy1 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-45: RDDatBy1 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7	$0_A0:7	MDQ8
6	$1_E2:7	MDQ9
5	$0_A1:1	MDQ10
4	$1_E3:2	MDQ11
3	$0_A1:2	MDQ12
2	$0_A1:6	MDQ13
1	$0_A1:5	MDQ14
0 (LSB)	$0_A1:4	MDQ15

Table 3–46 lists the channel assignments for the RDDatBy2 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-46: RDDatBy2 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7	$1_E3:1	MDQ16
6	$1_E3:5	MDQ17
5	$1_C2:4	MDQ18
4	$1_C2:5	MDQ19
3	$1_E3:3	MDQ20
2	$0_A2:0	MDQ21
1	$0_A2:2	MDQ22
0 (LSB)	$0_A2:3	MDQ23

Table 3–47 lists the channel assignments for the RDDatBy3 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-47: RDDatBy3 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7	$0_A2:5	MDQ24
6	$1_C2:7	MDQ25
5	$0_A3:2	MDQ26
4	$0_A3:4	MDQ27
3	$0_A2:6	MDQ28
2	$0_A3:0	MDQ29
1	$1_C3:4	MDQ30
0 (LSB)	$1_C3:3	MDQ31

Table 3–48 lists the channel assignments for the RDDatBy4 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-48: RDDatBy4 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7	$0_E2:4	MDQ32
6	$1_A2:5	MDQ33
5	$0_E2:6	MDQ34
4	$0_E3:1	MDQ35
3	$0_E2:3	MDQ36
2	$0_E2:5	MDQ37
1	$1_A2:7	MDQ38
0 (LSB)	$0_E3:0	MDQ39

Table 3–49 lists the channel assignments for the RDDatBy5 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-49: RDDatBy5 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7	$0_E3:2	MDQ40
6	$0_E3:3	MDQ41
5	$1_A3:3	MDQ42
4	$1_A3:6	MDQ43
3	$0_E3:4	MDQ44
2	$0_E3:6	MDQ45
1	$1_A3:7	MDQ46
0 (LSB)	$1_A3:2	MDQ47

Table 3–50 lists the channel assignments for the RDDatBy6 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-50: RDDatBy6 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7	$1_A3:5	MDQ48
6	$1_A0:0	MDQ49
5	$1_A0:5	MDQ50
4	$0_C3:4	MDQ51
3	$1_A0:1	MDQ52
2	$1_A0:2	MDQ53
1	$0_C3:3	MDQ54
0 (LSB)	$1_A0:3	MDQ55

Table 3–51 lists the channel assignments for the RDDatBy7 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-51: RDDatBy7 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
7	$0_C2:7	MDQ56
6	$0_C3:0	MDQ57
5	$1_A1:1	MDQ58
4	$1_A1:2	MDQ59
3	$1_A1:0	MDQ60
2	$0_C3:1	MDQ61
1	$0_C2:5	MDQ62
0 (LSB)	$0_C2:4	MDQ63

Table 3–52 lists the channel assignments for the WRDatBy0 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-52: WRDatBy0 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
8 (MSB)	$1_E2:3	MDM0
7	$1_E0:0	MDQ0_DM
6	$1_E0:1	MDQ1_DM
5	$0_D0:2	MDQ2_DM
4	$1_E0:4	MDQ3_DM
3	$0_D0:0	MDQ4_DM
2	$0_D0:1	MDQ5_DM
1	$0_D0:4	MDQ6_DM
0 (LSB)	$0_D0:3	MDQ7_DM

Table 3–53 lists the channel assignments for the WRDatBy1 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-53: WRDatBy1 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
8 (MSB)	$0_A1:7	MDM1
7	$0_D0:7	MDQ8_DM
6	$1_E0:7	MDQ9_DM
5	$0_D1:1	MDQ10_DM
4	$1_E1:2	MDQ11_DM
3	$0_D1:2	MDQ12_DM
2	$0_D1:6	MDQ13_DM
1	$0_D1:5	MDQ14_DM
0 (LSB)	$0_D1:4	MDQ15_DM

Table 3–54 lists the channel assignments for the WRDatBy2 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-54: WRDatBy2 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
8 (MSB)	$1_C2:2	MDM2
7	$1_E1:1	MDQ16_DM
6	$1_E1:5	MDQ17_DM
5	$1_C0:4	MDQ18_DM
4	$1_C0:5	MDQ19_DM
3	$1_E1:3	MDQ20_DM
2	$0_D2:0	MDQ21_DM
1	$0_D2:2	MDQ22_DM
0 (LSB)	$0_D2:3	MDQ23_DM

Table 3–55 lists the channel assignments for the WRDatBy3 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-55: WRDatBy3 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
8 (MSB)	$0_A3:1	MDM3
7	$0_D2:5	MDQ24_DM
6	$1_C0:7	MDQ25_DM
5	$0_D3:2	MDQ26_DM
4	$0_D3:4	MDQ27_DM
3	$0_D2:6	MDQ28_DM
2	$0_D3:0	MDQ29_DM
1	$1_C1:4	MDQ30_DM
0 (LSB)	$1_C1:3	MDQ31_DM

Table 3–56 lists the channel assignments for the WRDatBy4 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-56: WRDatBy4 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
8 (MSB)	$1_A3:0	MDM4
7	$0_E0:4	MDQ32_DM
6	$1_D2:5	MDQ33_DM
5	$0_E0:6	MDQ34_DM
4	$0_E1:1	MDQ35_DM
3	$0_E0:3	MDQ36_DM
2	$0_E0:5	MDQ37_DM
1	$1_D2:7	MDQ38_DM
0 (LSB)	$0_E1:0	MDQ39_DM

Table 3–57 lists the channel assignments for the WRDatBy5 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-57: WRDatBy5 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
8 (MSB)	$0_E3:7	MDM5
7	$0_E1:2	MDQ40_DM
6	$0_E1:3	MDQ41_DM
5	$1_D3:3	MDQ42_DM
4	$1_D3:6	MDQ43_DM
3	$0_E1:4	MDQ44_DM
2	$0_E1:6	MDQ45_DM
1	$1_D3:7	MDQ46_DM
0 (LSB)	$1_D3:2	MDQ47_DM

Table 3–58 lists the channel assignments for the WRDatBy6 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-58: WRDatBy6 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
8 (MSB)	$0_C3:6	MDM6
7	$1_D3:5	MDQ48_DM
6	$1_D0:0	MDQ49_DM
5	$1_D0:5	MDQ50_DM
4	$0_C1:4	MDQ51_DM
3	$1_D0:1	MDQ52_DM
2	$1_D0:2	MDQ53_DM
1	$0_C1:3	MDQ54_DM
0 (LSB)	$1_D0:3	MDQ55_DM

Table 3–59 lists the channel assignments for the WRDatBy7 group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-59: WRDatBy7 group assignments for 85XXDDR_RW support package

Bit order	Section:Channel	85XXDDR_RW support package channel name
8 (MSB)	$1_A0:7	MDM7
7	$0_C0:7	MDQ56_DM
6	$0_C1:0	MDQ57_DM
5	$1_D1:1	MDQ58_DM
4	$1_D1:2	MDQ59_DM
3	$1_D1:0	MDQ60_DM
2	$0_C1:1	MDQ61_DM
1	$0_C0:5	MDQ62_DM
0 (LSB)	$0_C0:4	MDQ63_DM

85XXLB Support Package Group Assignments

Tables 3–60 through 3–66 show the group assignments for the 85XXLB support package.

Table 3–60 lists the Address and Data group and the microprocessor signal to which each channel connects. By default, these groups are displayed in hexadecimal.

Table 3-60: Address and Data group assignments for 85XXLB support package

Bit order	Section:Channel	85XXLB support package channel name
31 (MSB)	A3:7	LAD0
30	A3:6	LAD1
29	A3:5	LAD2
28	A3:4	LAD3
27	A3:3	LAD4
26	A3:2	LAD5
25	A3:1	LAD6
24	A3:0	LAD7
23	A2:7	LAD8

Table 3-60: Address and Data group assignments for 85XXLB support package (Cont.)

Bit order	Section:Channel	85XXLB support package channel name
22	A2:6	LAD9
21	A2:5	LAD10
20	A2:4	LAD11
19	A2:3	LAD12
18	A2:2	LAD13
17	A2:1	LAD14
16	A2:0	LAD15
15	A1:7	LAD16
14	A1:6	LAD17
13	A1:5	LAD18
12	A1:4	LAD19
11	A1:3	LAD20
10	A1:2	LAD21
9	A1:1	LAD22
8	A1:0	LAD23
7	A0:7	LAD24
6	A0:6	LAD25
5	A0:5	LAD26
4	A0:4	LAD27
3	A0:3	LAD28
2	A0:2	LAD29
1	A0:1	LAD30
0 (LSB)	A0:0	LAD31

Table 3–61 lists the channel assignments for the BurstAddr group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-61: BurstAddr group assignments for 85XXLB support package

Bit order	Section:Channel	85XXLB support package channel name
4 (MSB)	D0:4	LA27
3	D0:3	LA28
2	D0:2	LA29
1	D0:1	LA30
0 (LSB)	D0:0	LA31

Table 3–62 lists the channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-62: Control group assignments for 85XXLB support package

Bit order	Section:Channel	85XXLB support package channel name
7 (MSB)	Clock:2	MDVAL
6	Clock:1	LGTA~/LGPL4/LUPWAIT/ LPBSE
5	Clock:0	LBCTL
4	D1:2	LSDA10/LGPL0
3	C2:3	LALE
2	C2:0	LSDRAS~/LBOE~/LGPL2
1	C2:1	LSDCAS~/LGPL3
0 (LSB)	C2:2	LSDWE~/LGPL1

Table 3–63 lists the channel assignments for the ChipSel group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-63: ChipSel group assignments for 85XXLB support package

Bit order	Section:Channel	85XXLB support package channel name
7 (MSB)	C3:7	LCS0~
6	C3:6	LCS1~
5	C3:5	LCS2~
4	C3:4	LCS3~
3	C3:3	LCS4~
2	C3:2	LCS5~
1	C3:1	LCS6~
0 (LSB)	C3:0	LCS7~

Table 3–64 lists the channel assignments for the Debug group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-64: Debug group assignments for 85XXLB support packages

Bit order	Section:Channel	85XXLB support package channel name
4 (MSB)	D1:7	MSRCID0
3	D1:6	MSRCID1
2	D1:5	MSRCID2
1	D1:4	MSRCID3
0 (LSB)	D1:3	MSRCID4

Table 3–65 lists the channel assignments for the DataMask group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-65: DataMask group assignments for 85XXLB support package

Bit order	Section:Channel	85XXLB support package channel name
3 (MSB)	C2:7	LSDDQM0/LWE0~/LBS0~
2	C2:6	LSDDQM1/LWE1~/LBS1~
1	C2:5	LSDDQM2/LWE2~/LBS2~
0 (LSB)	C2:4	LSDDQM3/LWE3~/LBS3~

Table 3–66 lists the channel assignmets for the UserDefined group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-66: UserDefined group assignments for 85XXLB support package

Bit order	Section:Channel	85XXLB support package channel name
4 (MSB)	D1:1	LGPL5
3	D0:5	LDP0/LCKE
2	D1:0	LDP1/TRIG_IN
1	D0:7	LDP2/TRIG_OUT
0 (LSB)	D0:6	LDP3

85XXLB_ALT Support Package Group Assignments

Tables 3–67 through 3–74 list the group assignments for the 85XXLB_ADS support package.

Table 3–67 lists the channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this group is displayed in hexadecimal.

Table 3-67: Address group assignments for 85XXLB_ALT support package

Bit order	Section:Channel	85XXLB_ALT support package channel name
31 (MSB)	A3:7	LA_D0
30	A3:6	LA_D1
29	A3:5	LA_D2

Table 3-67: Address group assignments for 85XXLB_ALT support package (Cont.)

Bit order	Section:Channel	85XXLB_ALT support package channel name
28	A3:4	LA_D3
27	A3:3	LA_D4
26	A3:2	LA_D5
25	A3:1	LA_D6
24	A3:0	LA_D7
23	A2:7	LA_D8
22	A2:6	LA_D9
21	A2:5	LA_D10
20	A2:4	LA_D11
19	A2:3	LA_D12
18	A2:2	LA_D13
17	A2:1	LA_D14
16	A2:0	LA_D15
15	A1:7	LA_D16
14	A1:6	LA_D17
13	A1:5	LA_D18
12	A1:4	LA_D19
11	A1:3	LA_D20
10	A1:2	LA_D21
9	A1:1	LA_D22
8	A1:0	LA_D23
7	A0:7	LA_D24
6	A0:6	LA_D25
5	A0:5	LA_D26
4	A0:4	LA_D27
3	A0:3	LA_D28
2	A0:2	LA_D29
1	A0:1	LA_D30
0 (LSB)	A0:0	LA_D31

Table 3–68 lists the channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this group is displayed in hexadecimal.

Table 3-68: Data group assignments for 85XXLB_ALT support package

Bit order	Section:Channel	85XXLB_ALT support package channel name
31 (MSB)	D3:7	LAD0
30	D3:6	LAD1
29	D3:5	LAD2
28	D3:4	LAD3
27	D3:3	LAD4
26	D3:2	LAD5
25	D3:1	LAD6
24	D3:0	LAD7
23	D2:7	LAD8
22	D2:6	LAD9
21	D2:5	LAD10
20	D2:4	LAD11
19	D2:3	LAD12
18	D2:2	LAD13
17	D2:1	LAD14
16	D2:0	LAD15
15	D1:7	LAD16
14	D1:6	LAD17
13	D1:5	LAD18
12	D1:4	LAD19
11	D1:3	LAD20
10	D1:2	LAD21
9	D1:1	LAD22
8	D1:0	LAD23
7	D0:7	LAD24
6	D0:6	LAD25
5	D0:5	LAD26
4	D0:4	LAD27
3	D0:3	LAD28
2	D0:2	LAD29
1	D0:1	LAD30
0 (LSB)	D0:0	LAD31

Table 3–69 lists the channel assignments for the BurstAddr group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-69: BurstAddr group assignments for 85XXLB_ALT support package

Bit order	Section:Channel	85XXLB_ALT support package channel name
4 (MSB)	C3: 2	LA27
3	C3: 1	LA28
2	C3: 0	LA29
1	C2: 7	LA30
0 (LSB)	C2: 6	LA31

Table 3–70 lists the channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-70: Control group assignments for 85XXLB_ALT support package

Bit order	Section:Channel	85XXLB_ALT support package channel name
11 (MSB)	Qual1	MDVAL
10	C3: 3	LSDDQM0/LWE0~
9	C3: 4	LSDDQM1/LWE1~
8	C3: 5	LSDDQM2/LWE2~
7	C3: 6	LSDDQM3/LWE3~
6	C2: 4	LGTA~
5	C3: 7	LBCTL
4	C2: 0	LSDA10/LGPL0
3	Clk1	LALE
2	C2: 2	LSDRAS~/LBOE~
1	C2: 3	LSDCAS~/LGPL3
0 (LSB)	C2: 1	LSDWE~LGPL1

Table 3–71 lists the channel assignments for the ChipSel group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-71: ChipSel group assignments for 85XXLB_ALT support package

Bit order	Section:Channel	85XXLB_ALT support package channel name
7 (MSB)	C0: 0	LCS0~
6	C0: 1	LCS1~
5	C0: 2	LCS2~
4	C0: 3	LCS3~
3	C0: 4	LCS4~
2	C0: 5	LCS5~
1	C0: 6	LCS6~
0 (LSB)	C0: 7	LCS7~

Table 3–72 lists the channel assignments for the Debug group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-72: Debug group assignments for 85XXLB_ALT support package

Bit order	Section:Channel	85XXLB_ALT support package channel name
4 (MSB)	C1: 3	MSRCID0
3	C1: 4	MSRCID1
2	C1: 5	MSRCID2
1	C1: 6	MSRCID3
0 (LSB)	C1: 7	MSRCID4

Table 3–73 lists the channel assignments for the DataMask group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-73: DataMask group assignments for 85XXLB_ALT support package

Bit order	Section:Channel	85XXLB_ALT support package channel name
3 (MSB)	C3: 3	LSDDQM0 /LWE0~
2	C3: 4	LSDDQM1 /LWE1~
1	C3: 5	LSDDQM2 /LWE2~
0 (LSB)	C3: 6	LSDDQM3 /LWE3~

Table 3–74 lists the channel assignments for the UserDefined group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-74: UserDefined group assignments for 85XXLB_ALT support package

Bit order	Section:Channel	85XXLB_ALT support package channel name
2 (MSB)	C2: 5	LGPL5
1	C1: 0	LDP0/LCKE
0 (LSB)	C1: 1	LDP2/TRIG_OUT

85XXLB_ADS Support Package Group Assignments

Tables 3–75 through 3–81 list the group assignments for the 85XXLB_ADS support package.

Table 3–75 lists the channel assignments for the Address and Data groups and the microprocessor signal to which each channel connects. By default, these groups are displayed in hexadecimal.

Table 3-75: Address and Data group assignments for 85XXLB_ADS support package

Bit order	Section:Channel	85XXLB_ADS support package channel name
31 (MSB)	A3:7	LAD0
30	A3:6	LAD1
29	A3:5	LAD2

Table 3-75: Address and Data group assignments for 85XXLB_ADS support package (Cont.)

Bit order	Section:Channel	85XXLB_ADS support package channel name
28	A3:4	LAD3
27	A3:3	LAD4
26	A3:2	LAD5
25	A3:1	LAD6
24	A3:0	LAD7
23	A2:7	LAD8
22	A2:6	LAD9
21	A2:5	LAD10
20	A2:4	LAD11
19	A2:3	LAD12
18	A2:2	LAD13
17	A2:1	LAD14
16	A2:0	LAD15
15	A1:7	LAD16
14	A1:6	LAD17
13	A1:5	LAD18
12	A1:4	LAD19
11	A1:3	LAD20
10	A1:2	LAD21
9	A1:1	LAD22
8	A1:0	LAD23
7	A0:7	LAD24
6	A0:6	LAD25
5	A0:5	LAD26
4	A0:4	LAD27
3	A0:3	LAD28
2	A0:2	LAD29
1	A0:1	LAD30
0 (LSB)	A0:0	LAD31

Table 3–76 lists the channel assignments for the BurstAddr group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-76: BurstAddr group assignments for 85XXLB_ADS support package

Bit order	Section:Channel	85XXLB_ADS support package channel name
4 (MSB)	C3: 2	LA27
3	C3: 1	LA28
2	C3: 0	LA29
1	C2: 7	LA30
0 (LSB)	C2: 6	LA31

Table 3–77 lists the channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-77: Control group assignments for 85XXLB_ADS support package

Bit order	Section:Channel	85XXLB_ADS support package channel name
11 (MSB)	Clk2	MDVAL
10	C3: 3	LSDDQM0/LWE0~
9	C3: 4	LSDDQM1/LWE1~
8	C3: 5	LSDDQM2/LWE2~
7	C3: 6	LSDDQM3/LWE3~
6	C2: 4	LGTA~
5	C3: 7	LBCTL
4	C2: 0	LSDA10/LGPL0
3	Clk1	LALE
2	C2: 2	LSDRAS~/LBOE~
1	C2: 3	LSDCAS~/LGPL3
0 (LSB)	C2: 1	LSDWE~LGPL1

Table 3–78 lists the channel assignments for the ChipSel group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-78: ChipSel group assignments for 85XXLB_ADS support package

Bit order	Section:Channel	85XXLB_ADS support package channel name
7 (MSB)	D0: 0	LCS0~
6	D0: 1	LCS1~
5	D0: 2	LCS2~
4	D0: 3	LCS3~
3	D0: 4	LCS4~
2	D0: 5	LCS5~
1	D0: 6	LCS6~
0 (LSB)	D0: 7	LCS7~

Table 3–79 lists the channel assignments for the Debug group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-79: Debug group assignments for 85XXLB_ADS support package

Bit order	Section:Channel	85XXLB_ADS support package channel name
4 (MSB)	D1: 3	MSRCID0
3	D1: 4	MSRCID1
2	D1: 5	MSRCID2
1	D1: 6	MSRCID3
0 (LSB)	D1: 7	MSRCID4

Table 3–80 lists the channel assignments for the DataMask group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-80: DataMask group assignments for 85XXLB_ADS support package

Bit order	Section:Channel	85XXLB_ADS support package channel name
3 (MSB)	C3: 3	LSDDQM0 /LWE0~
2	C3: 4	LSDDQM1 /LWE1~
1	C3: 5	LSDDQM2 /LWE2~
0 (LSB)	C3: 6	LSDDQM3 /LWE3~

Table 3–81 lists the channel assignments for the UserDefined group and the microprocessor signal to which each channel connects. By default, this group is not displayed.

Table 3-81: UserDefined group assignments for 85XXLB_ADS support package

Bit order	Section:Channel	85XXLB_ADS support package channel name
2 (MSB)	C2: 5	LGPL5
1	D1: 0	LDP0/LCKE
0 (LSB)	D1: 1	LDP2/TRIG_OUT

Clock and Qualifier Channel Assignments

Tables 3–82 through 3–86 list the channel assignments for the Clock and Qualifier probes for the MPC85XX interface, and the bus signal to which each channel connects.

Table 3-82: Clock and Qualifier channel assignments for 85XXDDR support package

Logic analyzer channel	85XXDDR support package channel name
Clk3	MCK2
Clk1	MCK1
Clk0	MCK0
Qual3	MWE~
C2:3	MCS0~
C2:2	MRAS~
C2:1	MCAS~
C2:0	MCS1~

Table 3-83: Clock and Qualifier channel assignments for 85XXDDR_RW support package

Logic analyzer channel	85XXDDR_RW support package channel name
$0_Clk3	MCK2
$0_Clk1	MCK1
$0_Clk0	MCK0
$0_Qual3	MWE~

Table 3-83: Clock and Qualifier channel assignments for 85XXDDR_RW support package (Cont.)

Logic analyzer channel	85XXDDR_RW support package channel name
$0_C2:3	MCS0~
$0_C2:2	MRAS~
$0_C2:1	MCAS~
$0_C2:0	MCS1~

Table 3-84: Clock and Qualifier channel assignments for 85XXLB suppor t package

Logic analyzer channel	85XXLB support package channel name
Clk3	LCLK0
Clk2	MDVAL
Clk1	LGTA~
C2:3	LALE
C2:2	LSDWE~/ LGPL1
C2:1	LSDCAS~/ LGPL3
C2:0	LSDRAS~/ LBOE~

Table 3-85: Clock and Qualifier channel assignments for 85XXLB_ALT support package

Logic analyzer channel	85XXLB_ALT support package channel name
Clk0	LCLK0
Clk1	LALE
C2:3	LSDCAS~/ LGPL3
C2:2	LSDRAS~/ LBOE~
C2:1	LSDWE~/ LGPL1
C2:0	MDVAL

Table 3-86: Clock and Qualifier channel assignments for 85XXLB_ADS support package

Logic analyzer channel	85XXLB_ADS support package channel name
Clk2	MDVAL
Clk1	LALE
Clk0	LCLK0
C2:3	LSDCAS~/ LGPL3
C2:2	LSDRAS~/ LBOE~
C2:1	LSDWE~/ LGPL1

Signals Required for Clocking and Disassembly

All signals other than those present in the group "UserDefined" are required for clocking and disassembly in all the five support packages 85XXDDR, 85XXDDR_RW, 85XXLB, 85XXLB_ALT, and 85XXLB_ADS.

Signals Not Required for Clocking and Disassembly

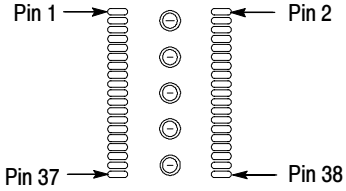
All signals present in the group "UserDefined" are not required for clocking and disassembly in all the five support packages 85XXDDR, 85XXDDR_RW, and 85XXLB, 85XXLB_ALT, and 85XXLB_ADS.

Signal Source To Probe Connections

For design purposes, you may need to make connections between the Signal Source and the P6434 or the P6860 Logic Analyzer Probe. Refer to the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction* manual, Tektronix part number 071-1059-XX and *P6434 Mass Termination Probe manual,* Tektronix part number 070-9793-XX, for more information on mechanical specifications. Tables 3–90 through 3–106 show the Signal Source to probe pin connections.

The recommended pin assignment is the AMP pin assignment for the 85XXLB support packages. See Table 3–87.

Table 3-87: Recommended pin assignments for a P6434 Mictor connector (component side)

Type of pin assignment	Comments
Recommended  **AMP Pin Assignment**	Recommended. You should use this pin assignment as it is the industry standard.

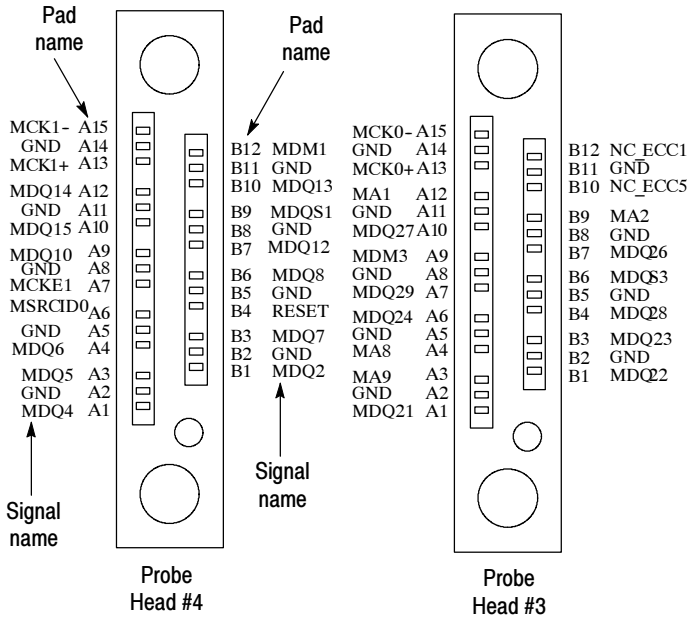


Figure 3-1: P6860 probe land footprint for MA-A0/A1 and MA-A2/A3

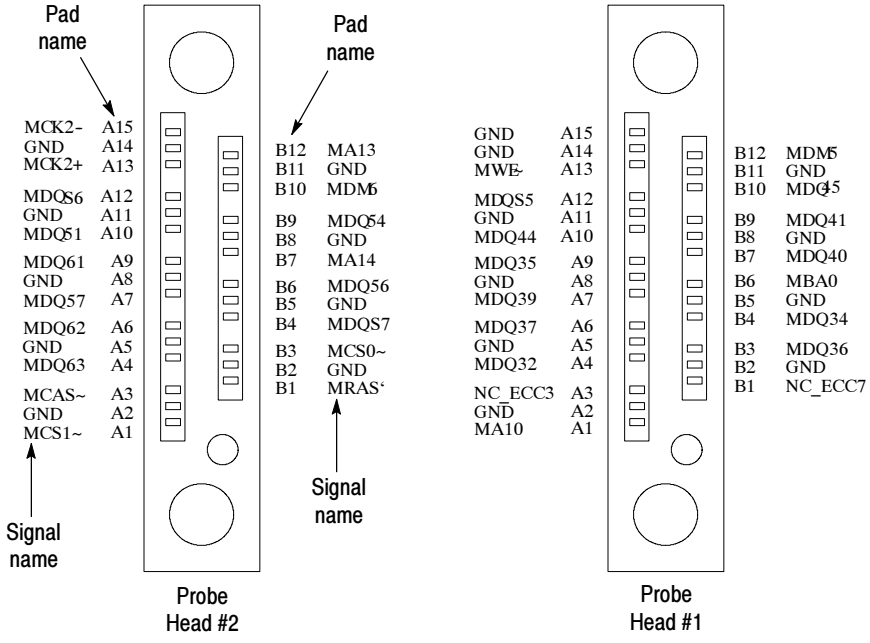


Figure 3-2: P6860 probe land footprint for MA-E2/E3 and SL-A0/A1

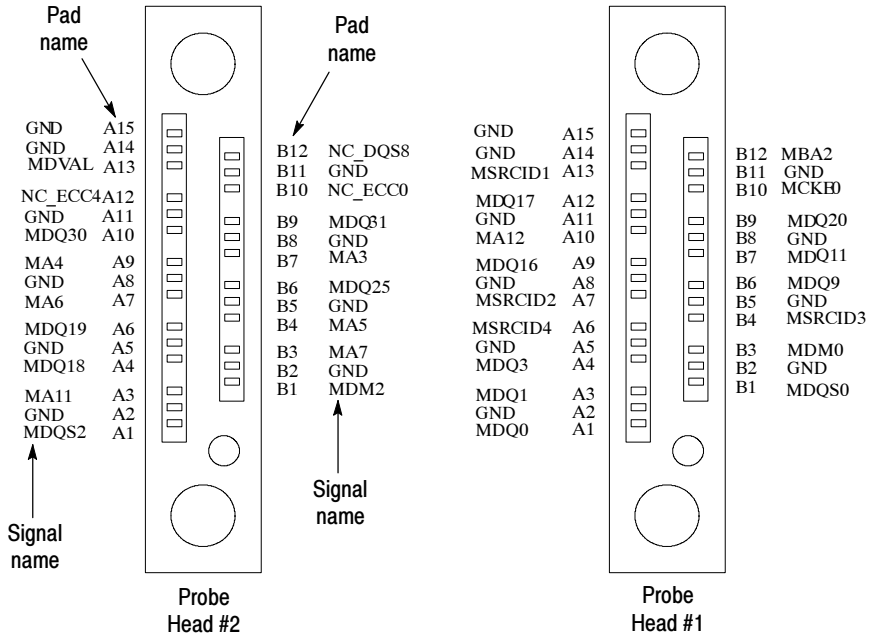


Figure 3-3: P6860 probe land footprint for SL-A0/A1 and SL-A2/A3

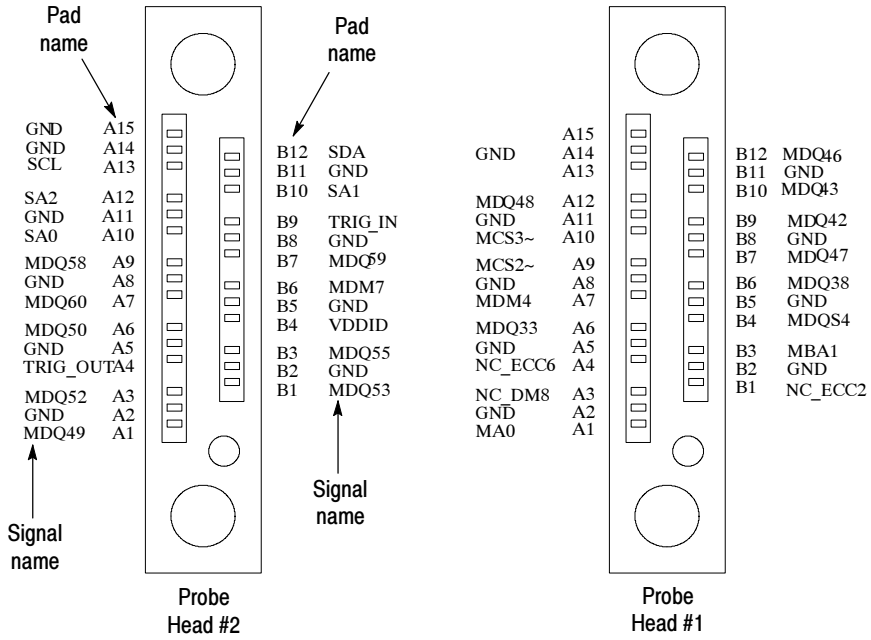


Figure 3-4: P6860 probe land footprint for SL-C2/C3 and SL-E2/E3

Table 3–88 lists the footprint to logic analyzer mapping for DDR support.

Table 3-88: Footprint to logic analyzer mapping for the 85XXDDR support package

Footprint name	Logic analyzer channel	Remarks
MA-A2/A3	A2/A3	Probe 1
SL-C2/C3	D2/D3	
MA-A0/A1	A0/A1	Probe 2
SL-E2/E3	D0/D1	
MA-C2/C3	C2/C3	Probe 3
SL-A0/A1	C0/C1	
MA-E2/E3	E2/E3	Probe 4
SL-A2/A3	E0/E1	

Table 3–89 lists the footprint to logic analyzer mapping for DDR support.

Table 3-89: Footprint to logic analyzer mapping for the 85XXDDR_RW support package

Footprint name	Logic analyzer channel	Remarks
MA-A2/A3	Master A2/A3	Probe 1
SL-C2/C3	Slave C2/C3	Probe 2
MA-A0/A1	Master A0/A1	Probe 3
SL-E2/E3	Slave E2/E3	Probe 4
MA-C2/C3	Master C2/C3	Probe 5
SL-A0/A1	Slave A0/A1	Probe 6
MA-E2/E3	Master E2/E3	Probe 7
SL-A2/A3	Slave A2/A3	Probe 8

P6860 Probe assignment footprint for 85XXLB support

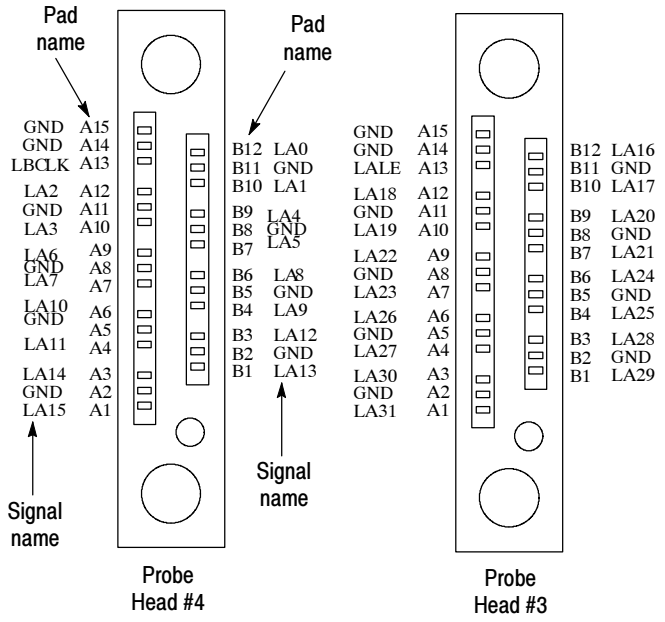


Figure 3-5: P6860 Probe land footprint for ELB-A2/A3 and ELB-A0/A1

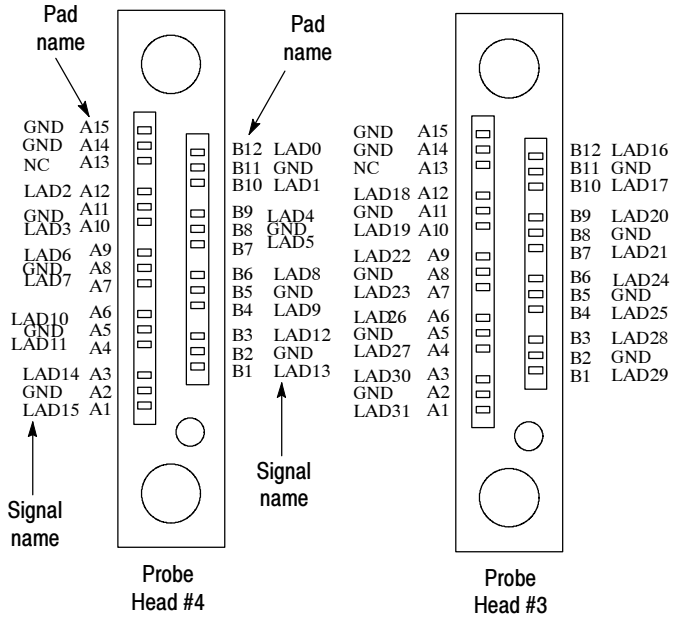


Figure 3-6: P6860 Probe land footprint for ELB-D2/D3 and ELB-D0/D1

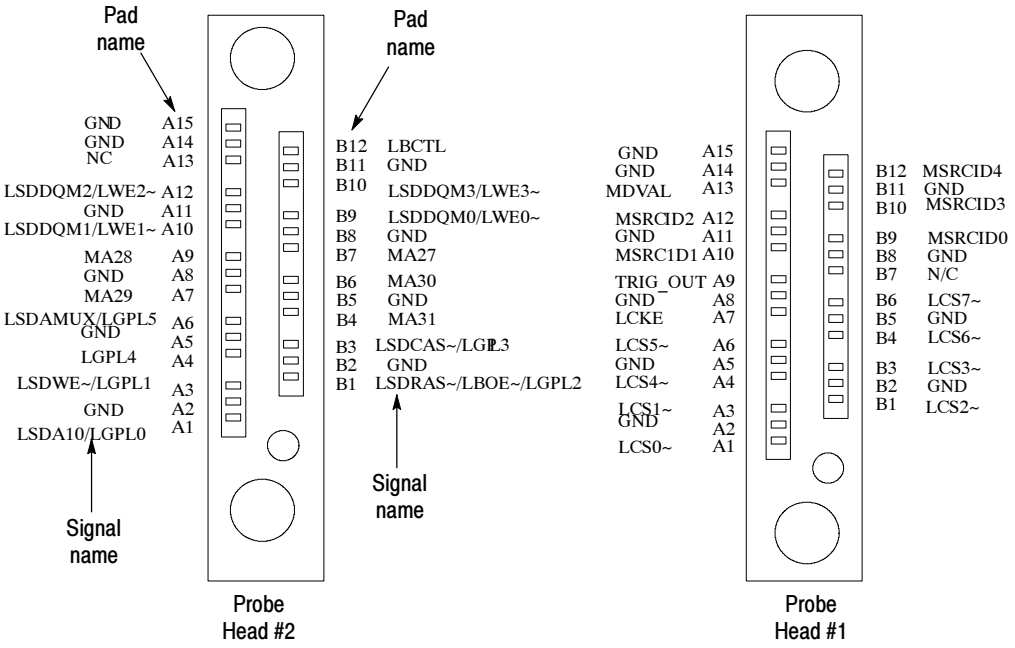


Figure 3-7: P6860 Probe land footprint for ELB-C2/C3 and ELB-C0/C1

Connections for the 85XXDDR Support Package

Tables 3–90 through 3–97 list the pin connections for the 85XXDDR support package.

Table 3–90 lists the MA–A2/A3 probe connections for the 85XXDDR support package.

Table 3-90: MA-A2/A3 probe connections for 85XXDDR support package

Logic analyzer channel	85XXDDR support package signal name	Pad number
CLK0-	MCK0~	A15
CLK0+	MCK0	A13
A3:7	ECC1	B12
A3:6	ECC5	B10
A3:5	MA1	A12
A3:4	MDQ27	A10
A3:3	MA2	B9
A3:2	MDQ26	B7
A3:1	MDM3	A9
A3:0	MDQ29	A7
A2:7	MDQS3	B6

Table 3-90: MA-A2/A3 probe connections for 85XXDDR support package (Cont.)

Logic analyzer channel	85XXDDR support package signal name	Pad number
A2:6	MDQ28	B4
A2:5	MDQ24	A6
A2:4	MA8	A4
A2:3	MDQ23	B3
A2:2	MDQ22	B1
A2:1	MA9	A3
A2:0	MDQ21	A1

Table 3–91 lists the MA–A0/A1 probe connections for the 85XXDDR support package.

Table 3-91: MA-A0/A1 probe connections for 85XXDDR support package

Logic analyzer channel	85XXDDR support package signal name	Pad number
CLK1-	MCK1~	A15
CLK+	MCK1	A13
A1:7	MDM1	B12
A1:6	MDQ13	B10
A1:5	MDQ14	A12
A1:4	MDQ15	A10
A1:3	MDQS1	B9
A1:2	MDQ12	B7
A1:1	MDQ10	A9
A1:0	MCKE1	A7
A0:7	MDQ8	B6
A0:6	RESET~	B4
A0:5	MSRCID0	A6
A0:4	MDQ6	A4
A0:3	MDQ7	B3
A0:2	MDQ2	B1
A0:1	MDQ5	A3
A0:0	MDQ4	A1

Table 3–92 MA–C2/C3 probe connections for the 85XXDDR support package.

Table 3-92: MA- C2/C3 probe connections for the 85XXDDR support package

Logic analyzer channel	85XXDDR support package signal name	Pad number
CLK3-	MCK2~	A15
CLK3+	MCK2	A13
C3:7	MA13	B12
C3:6	MDM6	B10
C3:5	MDQS6	A12
C3:4	MDQ51	A10
C3:3	MDQ54	B9
C3:2	MA14	B7
C3:1	MDQ61	A9
C3:0	MDQ57	A7
C2:7	MDQ56	B6
C2:6	MDQS7	B4
C2:5	MDQ62	A6
C2:4	MDQ63	A4
C2:3	MCS0~	B3
C2:2	MRAS~	B1
C2:1	MCAS~	A3
C2:0	MCS1~	A1

***NOTE**. The signal "MA14" is present only in MPC8560. This is an NC in MPC 8540.*

Table 3–93 lists the MA–E2/E3 probe connections for 85XXDDR support package.

Table 3-93: MA- E2/E3 probe connections for 85XXDDR support package

Logic analyzer channel	85XXDDR support package signal name	Pad number
Q3-	GND	A15
Q3+	MWE~	A13
E3:7	MDM5	B12

Table 3-93: MA-E2/E3 probe connections for 85XXDDR support package (Cont.)

Logic analyzer channel	85XXDDR support package signal name	Pad number
E3:6	MDQ45	B10
E3:5	MDQS5	A12
E3:4	MDQ44	A10
E3:3	MDQ41	B9
E3:2	MDQ40	B7
E3:1	MDQ35	A9
E3:0	MDQ39	A7
E2:7	MBA0	B6
E2:6	MDQ34	B4
E2:5	MDQ37	A6
E2:4	MDQ32	A4
E2:3	MDQ36	B3
E2:2	ECC7	B1
E2:1	ECC3	A3
E2:0	MA10	A1

Table 3–94 lists SL–A2/A3 probe connections for 85XXDDR support package.

Table 3-94: SL-A2/A3 probe connections for 85XXDDR support package

Logic analyzer channel	85XXDDR support package signal name	Pad number
Q2-	No Connection	A15
Q2+	No Connection	A13
E1:7	MDQ46	B12
E1:6	MDQ43	B10
E1:5	MDQ48	A12
E1:4	MCS3~	A10
E1:3	MDQ42	B9
E1:2	MDQ47	B7
E1:1	MCS2~	A9
E1:0	MDM4	A7
E0:7	MDQ38	B6
E0:6	MDQS4	B4

Table 3-94: SL-A2/A3 probe connections for 85XXDDR support package (Cont.)

Logic analyzer channel	85XXDDR support package signal name	Pad number
E0:5	MDQ33	A6
E0:4	ECC6	A4
E0:3	MBA1	B3
E0:2	ECC2	B1
E0:1	DM8	A3
E0:0	MA0	A1

Table 3-95 lists probe connections for 85XXDDR support package.

Table 3-95: SL-A0/A1 probe connections for 85XXDDR support package

Logic analyzer channel	85XXDDR support package signal name	Pad number
Q1-	GND	A15
Q1+	SCL	A13
C1:7	SDA	B12
C1:6	SA1	B10
C1:5	SA2	A12
C1:4	SA0	A10
C1:3	TRIG_IN	B9
C1:2	MDQ59	B7
C1:1	MDQ58	A9
C1:0	MDQ60	A7
C0:7	MDM7	B6
C0:6	VDDID	B4
C0:5	MDQ50	A6
C0:4	TRIG_OUT	A4
C0:3	MDQ55	B3
C0:2	MDQ53	B1
C0:1	MDQ52	A3
C0:0	MDQ49	A1

Table 3–96 lists the SL–C2/C3 probe connections for 85XXDDR support package.

Table 3-96: SL-C2/C3 probe connections for 85XXDDR support package

Logic analyzer channel	85XXDDR support package signal name	Pad number
Q0-	GND	A15
Q0+	MDVAL	A13
D3:7	DQS8	B12
D3:6	ECC0	B10
D3:5	ECC4	A12
D3:4	MDQ30	A10
D3:3	MDQ31	B9
D3:2	MA3	B7
D3:1	MA4	A9
D3:0	MA6	A7
D2:7	MDQ25	B6
D2:6	MA5	B4
D2:5	MDQ19	A6
D2:4	MDQ18	A4
D2:3	MA7	B3
D2:2	MDM2	B1
D2:1	MA11	A3
D2:0	MDQS2	A1

Table 3–97 lists SL–E2/E3 probe connections for 85XXDDR support package.

Table 3-97: SL-E2/E3 probe connections for 85XXDDR support package

Logic analyzer channel	85XXDDR support package signal name	Pad number
CLK2-	GND	A15
CLK2+	MSRCID1	A13
D1:7	MBA2	B12
D1:6	MCKE0	B10
D1:5	MDQ17	A12
D1:4	MA12	A10
D1:3	MDQ20	B9

Table 3-97: SL-E2/E3 probe connections for 85XXDDR support package (Cont.)

Logic analyzer channel	85XXDDR support package signal name	Pad number
D1:2	MDQ11	B7
D1:1	MDQ16	A9
D1:0	MSRCID2	A7
D0:7	MDQ9	B6
D0:6	MSRCID3	B4
D0:5	MSRCID4	A6
D0:4	MDQ3	A4
D0:3	MDM0	B3
D0:2	MDQS0	B1
D0:1	MDQ1	A3
D0:0	MDQ0	A1

Connections for the 85XXDDR_RW Support Package

Tables 3–98 through 3–105 list the pin connections for the 85XXDDR_RW support package.

Table 3–98 lists MA–A2/A3 probe connections for the 85XXDDR_RW support package.

Table 3-98: MA-A2/A3 probe connections for 85XXDDR_RW support package

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$0_CLK0-	MCK0~	A15
$0_CLK0+	MCK0	A13
$0_A3:7	ECC1	B12
$0_A3:6	ECC5	B10
$0_A3:5	MA1	A12
$0_A3:4	MDQ27	A10
$0_A3:3	MA2	B9
$0_A3:2	MDQ26	B7
$0_A3:1	MDM3	A9
$0_A3:0	MDQ29	A7
$0_A2:7	MDQS3	B6
$0_A2:6	MDQ28	B4
$0_A2:5	MDQ24	A6
$0_A2:4	MA8	A4
$0_A2:3	MDQ23	B3
$0_A2:2	MDQ22	B1
$0_A2:1	MA9	A3
$0_A2:0	MDQ21	A1

Table 3–99 lists MA–A0/A1 probe connections for 85XXDDR_RW support package.

Table 3-99: MA-A0/A1 probe connections for 85XXDDR_RW support package

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$0_CLK1-	MCK1~	A15
$0_CLK+	MCK1	A13

Table 3-99: MA-A0/A1 probe connections for 85XXDDR_RW support package (Cont.)

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$0_A1:7	MDM1	B12
$0_A1:6	MDQ13	B10
$0_A1:5	MDQ14	A12
$0_A1:4	MDQ15	A10
$0_A1:3	MDQS1	B9
$0_A1:2	MDQ12	B7
$0_A1:1	MDQ10	A9
$0_A1:0	MCKE1	A7
$0_A0:7	MDQ8	B6
$0_A0:6	RESET~	B4
$0_A0:5	MSRCID0	A6
$0_A0:4	MDQ6	A4
$0_A0:3	MDQ7	B3
$0_A0:2	MDQ2	B1
$0_A0:1	MDQ5	A3
$0_A0:0	MDQ4	A1

Table 3–100 lists MA–C2/C3 probe connections for 85XXDDR_RW support package.

Table 3-100: MA-C2/C3 probe connections for 85XXDDR_RW support package

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$0_CLK3-	MCK2~	A15
$0_CLK3+	MCK2	A13
$0_C3:7	MA13	B12
$0_C3:6	MDM6	B10
$0_C3:5	MDQS6	A12
$0_C3:4	MDQ51	A10
$0_C3:3	MDQ54	B9
$0_C3:2	MA14	B7
$0_C3:1	MDQ61	A9

Table 3-100: MA-C2/C3 probe connections for 85XXDDR_RW support package (Cont.)

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$0_C3:0	MDQ57	A7
$0_C2:7	MDQ56	B6
$0_C2:6	MDQS7	B4
$0_C2:5	MDQ62	A6
$0_C2:4	MDQ63	A4
$0_C2:3	MCS0~	B3
$0_C2:2	MRAS~	B1
$0_C2:1	MCAS~	A3
$0_C2:0	MCS1~	A1

***NOTE**. The signal "MA14" is present only in MPC8560. This is an NC in MPC8540.*

Table 3-101 lists MA-E2/E3 probe connections for 85XXDDR_RW support package.

Table 3-101: MA-E2/E3 probe connections for 85XXDDR_RW support package

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$0_Q3-	GND	A15
$0_Q3+	MWE~	A13
$0_E3:7	MDM5	B12
$0_E3:6	MDQ45	B10
$0_E3:5	MDQS5	A12
$0_E3:4	MDQ44	A10
$0_E3:3	MDQ41	B9
$0_E3:2	MDQ40	B7
$0_E3:1	MDQ35	A9
$0_E3:0	MDQ39	A7
$0_E2:7	MBA0	B6
$0_E2:6	MDQ34	B4
$0_E2:5	MDQ37	A6

Table 3-101: MA-E2/E3 probe connections for 85XXDDR_RW support package (Cont.)

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$0_E2:4	MDQ32	A4
$0_E2:3	MDQ36	B3
$0_E2:2	ECC7	B1
$0_E2:1	ECC3	A3
$0_E2:0	MA10	A1

Table 3-102 lists SL-A2./A3 probe connections for 85XXDDR_RW support package.

Table 3-102: SL-A2/A3 probe connections for 85XXDDR_RW support package

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$1_CLK0-	No Connection	A15
$1_CLK0+	No Connection	A13
$1_A3:7	MDQ46	B12
$1_A3:6	MDQ43	B10
$1_A3:5	MDQ48	A12
$1_A3:4	MCS3~	A10
$1_A3:3	MDQ42	B9
$1_A3:2	MDQ47	B7
$1_A3:1	MCS2~	A9
$1_A3:0	MDM4	A7
$1_A2:7	MDQ38	B6
$1_A2:6	MDQS4	B4
$1_A2:5	MDQ33	A6
$1_A2:4	ECC6	A4
$1_A2:3	MBA1	B3
$1_A2:2	ECC2	B1
$1_A2:1	DM8	A3
$1_A2:0	MA0	A1

Table 3–103 lists SL–A0/A1 probe connections for 85XXDDR_RW support package.

Table 3-103: SL-A0/A1 probe connections for 85XXDDR_RW support package

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$1_CLK1-	GND	A15
$1_CLK1+	SCL	A13
$1_A1:7	SDA	B12
$1_A1:6	SA1	B10
$1_A1:5	SA2	A12
$1_A1:4	SA0	A10
$1_A1:3	TRIG_IN	B9
$1_A1:2	MDQ59	B7
$1_A1:1	MDQ58	A9
$1_A1:0	MDQ60	A7
$1_A0:7	MDM7	B6
$1_A0:6	VDDID	B4
$1_A0:5	MDQ50	A6
$1_A0:4	TRIG_OUT	A4
$1_A0:3	MDQ55	B3
$1_A0:2	MDQ53	B1
$1_A0:1	MDQ52	A3
$1_A0:0	MDQ49	A1

Table 3–104 lists SL–C2/C3 probe connections for 85XXDDR_RW support package.

Table 3-104: SL-C2/C3 probe connections for 85XXDDR_RW support package

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$1_CLK3-	GND	A15
$1_CLK3+	MDVAL	A13
$1_C3:7	DQS8	B12
$1_C3:6	ECC0	B10

Table 3-104: SL-C2/C3 probe connections for 85XXDDR_RW support package (Cont.)

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$1_C3:5	ECC4	A12
$1_C3:4	MDQ30	A10
$1_C3:3	MDQ31	B9
$1_C3:2	MA3	B7
$1_C3:1	MA4	A9
$1_C3:0	MA6	A7
$1_C2:7	MDQ25	B6
$1_C2:6	MA5	B4
$1_C2:5	MDQ19	A6
$1_C2:4	MDQ18	A4
$1_C2:3	MA7	B3
$1_C2:2	MDM2	B1
$1_C2:1	MA11	A3
$1_C2:0	MDQS2	A1

Table 3–105 lists SL–E2/E3 probe connections for 85XXDDR_RW support package.

Table 3-105: SL-E2/E3 probe connections for 85XXDDR_RW support package

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$1_Q3-	GND	A15
$1_Q3+	MSRCID1	A13
$1_E3:7	MBA2	B12
$1_E3:6	MCKE0	B10
$1_E3:5	MDQ17	A12
$1_E3:4	MA12	A10
$1_E3:3	MDQ20	B9
$1_E3:2	MDQ11	B7
$1_E3:1	MDQ16	A9
$1_E3:0	MSRCID2	A7
$1_E2:7	MDQ9	B6

Table 3-105: SL-E2/E3 probe connections for 85XXDDR_RW support package (Cont.)

Logic analyzer channel	85XXDDR_RW support package signal name	Pad number
$1_E2:6	MSRCID3	B4
$1_E2:5	MSRCID4	A6
$1_E2:4	MDQ3	A4
$1_E2:3	MDM0	B3
$1_E2:2	MDQS0	B1
$1_E2:1	MDQ1	A3
$1_E2:0	MDQ0	A1

Connections for the 85XXLB Support Package

Tables 3–106 through 3–111 list the pin connections for the 85XXLB support package.

Table 3–106 lists the Mictor A pin connetions for 85XXLB support package.

Table 3-106: Mictor A connections for 85XXLB support package

Logic analyzer channel	85XXLB support package signal name	AMP Mictor A pin number
CLK0	LBCTL	5
A3:7	LAD0 (MSB)	7
A3:6	LAD1	9
A3:5	LAD2	11
A3:4	LAD3	13
A3:3	LAD4	15
A3:2	LAD5	17
A3:1	LAD6	19
A3:0	LAD7	21
A2:7	LAD8	23
A2:6	LAD9	25
A2:5	LAD10	27
A2:4	LAD11	29
A2:3	LAD12	31
A2:2	LAD13	33
A2:1	LAD14	35
A2:0	LAD15	37
CLK1	LGTA~/LGPL4/LUPWAIT/LPBSE	6
A1:7	LAD16	8
A1:6	LAD17	10
A1:5	LAD18	12
A1:4	LAD19	14
A1:3	LAD20	16
A1:2	LAD21	18
A1:1	LAD22	20
A1:0	LAD23	22
A0:7	LAD24	24
A0:6	LAD25	26
A0:5	LAD26	28
A0:4	LAD27	30

Table 3-106: Mictor A connections for 85XXLB support package (Cont.)

Logic analyzer channel	85XXLB support package signal name	AMP Mictor A pin number
A0:3	LAD28	32
A0:2	LAD29	34
A0:1	LAD30	36
A0:0	LAD31 (LSB)	38

Table 3–107 lists Mictor C connections for the 85XXLB support package.

Table 3-107: Mictor C connections for 85XXLB support package (Probe #3)

Logic analyzer channel	85XXLB support package signal name	AMP Mictor C pin number
CLK3	LCLK0	5
C3:7	LCS0~	7
C3:6	LCS1~	9
C3:5	LCS2~	11
C3:4	LCS3~	13
C3:3	LCS4~	15
C3:2	LCS5~	17
C3:1	LCS6~	19
C3:0	LCS7~	21
C2:7	LSDDQM0/LWE0~/LBS0~	23
C2:6	LSDDQM1/LWEl~/LBS1~	25
C2:5	LSDDQM2/LWE2~/LBS2~	27
C2:4	LSDDQM3/LWE3~/LBS3~	29
C2:3	LALE	31
C2:2	LSDWE~/LGPL1	33
C2:1	LSDCAS~/LGPL3	35
C2:0	LSDRAS~/LBOE~/LGPL2	37

Table 3–108 lists Mictor D connections for the 85XXLB support package.

Table 3-108: Mictor D connections for 85XXLB support package (Probe #3)

Logic analyzer channel	85XXLB support package signal name	AMP Mictor D pin number
CLK2	MDVAL	6
D1:7	MSRCID0	8
D1:6	MSRCID1	10
D1:5	MSRCID2	12
D1:4	MSRCID3	14
D1:3	MSRCID4	16
D1:2	LSDA10/ LGPL0	18
D1:1	LSDAMUX/LGPL5	20
D1:0	LDP1/TRIG_IN	22
D0:7	LDP2/TRIG_OUT	24
D0:6	LDP3	26
D0:5	LDP0/LCKE	28
D0:4	LA27	30
D0:3	LA28	32
D0:2	LA29	34
D0:1	LA30	36
D0:0	LA31	38

Table 3–109 lists A3/A2 connections using P6860 probe for the 85XXLB support package.

Table 3-109: A3/A2 connections using P6860 probe for 85XXLB support package

Logic analyzer channel	85XXLB support package signal name	Pad number
CLK0-	GND	A15
CLK0+	LBCTL	A13
A3:7	LAD0	B12
A3:6	LAD1	B10
A3:5	LAD2	A12
A3:4	LAD3	A10
A3:3	LAD4	B9

Table 3-109: A3/A2 connections using P6860 probe for 85XXLB support package (Cont.)

Logic analyzer channel	85XXLB support package signal name	Pad number
A3:2	LAD5	B7
A3:1	LAD6	A9
A3:0	LAD7	A7
A2:7	LAD8	B6
A2:6	LAD9	B4
A2:5	LAD10	A6
A2:4	LAD11	A4
A2:3	LAD12	B3
A2:2	LAD13	B1
A2:1	LAD14	A3
A2:0	LAD15	A1

Table 3-110 lists C3/C2 connections using P6860 probe for the 85XXLB support package.

Table 3-110: C3/C2 connections using P6860 probe for 85XXLB support package

Logic analyzer channel	85XXLB support package signal name	Pad number
CLK3-	GND	A15
CLK3+	LCLK0	A13
C3:7	LCS0	B12
C3:6	LCS1	B10
C3:5	LCS2	A12
C3:4	LCS3	A10
C3:3	LCS4	B9
C3:2	LCS5	B7
C3:1	LCS6	A9
C3:0	LCS7	A7
C2:7	LSDDQM0/LWE0~/LBS0~	B6
C2:6	LSDDQM1/LWE1~/LBS1~	B4
C2:5	LSDDQM2/LWE2~/LBS2~	A6
C2:4	LSDDQM3/LWE3~/LBS3~	A4

Table 3-110: C3/C2 connections using P6860 probe for 85XXLB support package (Cont.)

Logic analyzer channel	85XXLB support package signal name	Pad number
C2:3	LALE	B3
C2:2	LSDWE~/LGPL1	B1
C2:1	LSDCAS~/LGPL3	A3
C2:0	LSDRAS~/LBOE~/LGPL2	A1

Table 3-111 lists A1/A0 connections using P6860 probe for the 85XXLB support package.

Table 3-111: A1/A0 connections using P6860 probe for 85XXLB support package

Logic analyzer channel	85XXLB support package signal name	Pad number
CLK1-	GND	A15
CLK1+	LGTA~/LGPL4LUPWAITLPBSE	A13
A1:7	LAD16	B12
A1:6	LAD17	B10
A1:5	LAD18	A12
A1:4	LAD19	A10
A1:3	LAD20	B9
A1:2	LAD21	B7
A1:1	LAD22	A9
A1:0	LAD23	A7
A0:7	LAD24	B6
A0:6	LAD25	B4
A0:5	LAD26	A6
A0:4	LAD27	A4
A0:3	LAD28	B3
A0:2	LAD29	B1
A0:1	LAD30	A3
A0:0	LAD31	A1
CLK2-	GND	A15
CLK2+	MDVAL	A13
D1:7	MSRCID0	B12

Table 3-111: A1/A0 connections using P6860 probe for 85XXLB support package (Cont.)

Logic analyzer channel	85XXLB support package signal name	Pad number
D1:6	MSRCID1	B10
D1:5	MSRCID2	A12
D1:4	MSRCID3	A10
D1:3	MSRCID4	B9
D1:2	LSDA10 /LGPL0	B7
D1:1	LSDAMUX/LGPL5	A9
D1:0	LDP1/TRIG_IN	A7
D0:7	LDP2/TRIG_OUT	B6
D0:6	LDP3	B4
D0:5	LDP0/LCKE	A6
D0:4	LA27	A4
D0:3	LA28	B3
D0:2	LA29	B1
D0:1	LA30	A3
D0:0	LA31	A1

Connections for 85XXLB_ALT Support Package

Tables 3–112 through 3–120 list the probe connections for the 85XXLB_ALT support package.

Table 3–112 lists the address connections for 85XXLB_ALT support package.

Table 3-112: Address connections for 85XXLB_ALT support package

Logic analyzer channel	85XXLB_ALT support package signal name	Tek mictor pin number	Amp mictor pin number
CLOCK:0	LBCLK	3	5
A3:7	LA0	4	7
A3:6	LA1	5	9
A3:5	LA2	6	11
A3:4	LA3	7	13
A3:3	LA4	8	15
A3:2	LA5	9	17
A3:1	LA6	10	19
A3:0	LA7	11	21

Table 3-112: Address connections for 85XXLB_ALT support package (Cont.)

Logic analyzer channel	85XXLB_ALT support package signal name	Tek mictor pin number	Amp mictor pin number
A2:7	LA8	12	23
A2:6	LA9	13	25
A2:5	LA10	14	27
A2:4	LA11	15	29
A2:3	LA12	16	31
A2:2	LA13	17	33
A2:1	LA14	18	35
A2:0	LA15	19	37
CLOCK:1	LALE	36	6
A1:7	LA16	35	8
A1:6	LA17	34	10
A1:5	LA18	33	12
A1:4	LA19	32	14
A1:3	LA20	31	16
A1:2	LA21	30	18
A1:1	LA22	29	20
A1:0	LA23	28	22
A0:7	LA24	27	24
A0:6	LA25	26	26
A0:5	LA26	25	28
A0:4	LA27	24	30
A0:3	LA28	23	32
A0:2	LA29	22	34
A0:1	LA30	21	36
A0:0	LA31	20	38

Table 3–113 lists data connections for 85XXLB_ALT support packages.

Table 3-113: Data connections for 85XXLB_ALT support package

Logic analyzer channel	85XXLB_ALT support package signal name	TEK mictor pin number	AMP mictor pin number
Qual:0	No Signal	3	5
D3:7	LAD0	4	7
D3:6	LAD1	5	9
D3:5	LAD2	6	11
D3:4	LAD3	7	13
D3:3	LAD4	8	15
D3:2	LAD5	9	17
D3:1	LAD6	10	19
D3:0	LAD7	11	21
D2:7	LAD8	12	23
D2:6	LAD9	13	25
D2:5	LAD10	14	27
D2:4	LAD11	15	29
D2:3	LAD12	16	31
D2:2	LAD13	17	33
D2:1	LAD14	18	35
D2:0	LAD15	19	37
CLOCK:2	No Signal	36	6
D1:7	LAD16	35	8
D1:6	LAD17	34	10
D1:5	LAD18	33	12
D1:4	LAD19	32	14
D1:3	LAD20	31	16
D1:2	LAD21	30	18
D1:1	LAD22	29	20
D1:0	LAD23	28	22
D0:7	LAD24	27	24
D0:6	LAD25	26	26
D0:5	LAD26	25	28
D0:4	LAD27	24	30
D0:3	LAD28	23	32

Table 3-113: Data connections for 85XXLB_ALT support package (Cont.)

Logic analyzer channel	85XXLB_ALT support package signal name	TEK mictor pin number	AMP mictor pin number
D0:2	LAD29	22	34
D0:1	LAD30	21	36
D0:0	LAD31	20	38

Table 3–114 lists the control connections for 85XXLB_ALT support package.

Table 3-114: Control connections for 85XXLB support package

Logic analyzer channel	85XXLB_ALT support package signal name	TEK mictor pin number	AMP mictor pin number
CLOCK:3	No Connection	3	5
C3:7	LBCTL	4	7
C3:6	LSDDQM3/LWE3~	5	9
C3:5	LSDDQM2/LWE2~	6	11
C3:4	LSDDQM1/LWE1~	7	13
C3:3	LSDDQM0/LWE0~	8	15
C3:2	MA27	9	17
C3:1	MA28	10	19
C3:0	MA29	11	21
C2:7	MA30	12	23
C2:6	MA31	13	25
C2:5	LSDAMUX/LGPL5	14	27
C2:4	LGPL4	15	29
C2:3	LSDCAS~/LGPL3	16	31
C2:2	LSDRAS~/LBOE~/LGPL2	17	33
C2:1	LSDWE~/LGPL1	18	35
C2:0	LSDA10/LGPL0	19	37
Qual:1	MDVAL	36	6
C1:7	MSRCID4	35	8
C1:6	MSRCID3	34	10
C1:5	MSRCID2	33	12
C1:4	MSRCID1	32	14

Table 3-114: Control connections for 85XXLB support package (Cont.)

Logic analyzer channel	85XXLB_ALT support package signal name	TEK mictor pin number	AMP mictor pin number
C1:3	MSRCID0	31	16
C1:2	No Connection	30	18
C1:1	TRIG_OUT	29	20
C1:0	LCKE	28	22
C0:7	LCS7~	27	24
C0:6	LCS6~	26	26
C0:5	LCS5~	25	28
C0:4	LCS4~	24	30
C0:3	LCS3~	23	32
C0:2	LCS2~	22	34
C0:1	LCS1~	21	36
C0:0	LCS0~	20	38

Table 3–115 lists the ELB–A2/A3 probe head assignment for the 85XXLB_ALT support package.

Table 3-115: ELB-A2/A3 probe head assignment for 85XXLB_ALT support package

Logic analyzer channel	85XXLB_ALT support package signal name	P6860 probe pad number
Clock:0-	GND	A15
Clock:0+	LBCLK	A13
A3:7	LA0	B12
A3:6	LA1	B10
A3:5	LA2	A12
A3:4	LA3	A10
A3:3	LA4	B9
A3:2	LA5	B7
A3:1	LA6	A9
A3:0	LA7	A7
A2:7	LA8	B6
A2:6	LA9	B4
A2:5	LA10	A6
A2:4	LA11	A4
A2:3	LA12	B3
A2:2	LA13	B1
A2:1	LA14	A3
A2:0	LA15	A1

Table 3–116 lists the ELB–A0/A1 probe head assignment for the 85XXLB_ALT support package.

Table 3-116: ELB-A0/A1 probe head assignment for 85XXLB_ALT support package

Logic analyzer channel	85XXLB_ALT support package signal name	P6860 probe pad number
Clock:1-	GND	A15
Clock:1+	LALE	A13
A1:7	LA16	B12
A1:6	LA17	B10
A1:5	LA18	A12
A1:4	LA19	A10
A1:3	LA20	B9
A1:2	LA21	B7
A1:1	LA22	A9
A1:0	LA23	A7
A0:7	LA24	B6
A0:6	LA25	B4
A0:5	LA26	A6
A0:4	LA27	A4
A0:3	LA28	B3
A0:2	LA29	B1
A0:1	LA30	A3
A0:0	LA31	A1

Table 3–117 lists the ELB–D2/D3 probe head assignment for the 85XXLB_ALT support package.

Table 3-117: ELB-D2/D3 probe head assignment for 85XXLB_ALT support package

Logic analyzer channel	85XXLB_ALT support package signal name	P6860 probe pad number
Q0-	GND	A15
Q0+	No Signal	A13
D3:7	LAD0	B12

Table 3-117: ELB-D2/D3 probe head assignment for 85XXLB_ALT support package (Cont.)

Logic analyzer channel	85XXLB_ALT support package signal name	P6860 probe pad number
D3:6	LAD1	B10
D3:5	LAD2	A12
D3:4	LAD3	A10
D3:3	LAD4	B9
D3:2	LAD5	B7
D3:1	LAD6	A9
D3:0	LAD7	A7
D2:7	LAD8	B6
D2:6	LAD9	B4
D2:5	LAD10	A6
D2:4	LAD11	A4
D2:3	LAD12	B3
D2:2	LAD13	B1
D2:1	LAD14	A3
D2:0	LAD15	A1

Table 3–118 lists the ELB–A0/A1 probe head assignment for the 85XXLB_ALT support package.

Table 3-118: ELB-A0/A1 probe head assignment for 85XXLB_ALT support package

Logic analyzer channel	85XXLB_ALT support package signal name	P6860 probe pad number
Clock:2-	GND	A15
Clock:2+	No Signal	A13
D1:7	LAD16	B12
D1:6	LAD17	B10
D1:5	LAD18	A12
D1:4	LAD19	A10
D1:3	LAD20	B9
D1:2	LAD21	B7
D1:1	LAD22	A9

Table 3-118: ELB-A0/A1 probe head assignment for 85XXLB_ALT support package (Cont.)

Logic analyzer channel	85XXLB_ALT support package signal name	P6860 probe pad number
D1:0	LAD23	A7
D0:7	LAD24	B6
D0:6	LAD25	B4
D0:5	LAD26	A6
D0:4	LAD27	A4
D0:3	LAD28	B3
D0:2	LAD29	B1
D0:1	LAD30	A3
D0:0	LAD31	A1

Table 3–119 lists the ELB–C2/C3 probe head assignment for the 85XXLB_ALT support package.

Table 3-119: ELB-C2/C3 probe head assignment for 85XXLB_ALT support package

Logic analyzer channel	85XXLB_ALT support package signal name	P6860 probe pad number
Clock:3-	GND	A15
Clock:3+	No Connection	A13
C3:7	LBCTL	B12
C3:6	LSDDQM3/LWE3~	B10
C3:5	LSDDQM2/LWE2~	A12
C3:4	LSDDQM1/LWE1~	A10
C3:3	LSDDQM0/LWE0~	B9
C3:2	MA27	B7
C3:1	MA28	A9
C3:0	MA29	A7
C2:7	MA30	B6
C2:6	MA31	B4
C2:5	LSDAMUX/LGPL5	A6
C2:4	LGPL4	A4
C2:3	LSDCAS~/LGPL3	B3

Table 3-119: ELB-C2/C3 probe head assignment for 85XXLB_ALT support package (Cont.)

Logic analyzer channel	85XXLB_ALT support package signal name	P6860 probe pad number
C2:2	LSDRAS~/LBOE~/LGPL2	B1
C2:1	LSDWE~/LGPL1	A3
C2:0	LSDA10/LGPL0	A1

Table 3-120 lists the ELB-D0/D1 probe head assignment for the 85XXLB_ALT support package.

Table 3-120: ELB-D0/D1 probe head assignment for 85XXLB_ALT support package

Logic analyzer channel	85XXLB_ALT support package signal name	P6860 probe pad number
Q1-	GND	A15
Q1+	MDVAL	A13
C1:7	MSRCID4	B12
C1:6	MSRCID3	B10
C1:5	MSRCID2	A12
C1:4	MSRCID1	A10
C1:3	MSRCID0	B9
C1:2	No Connection	B7
C1:1	TRIG_OUT	A9
C1:0	LCKE	A7
C0:7	LCS7~	B6
C0:6	LCS6~	B4
C0:5	LCS5~	A6
C0:4	LCS4~	A4
C0:3	LCS3~	B3
C0:2	LCS2~	B1
C0:1	LCS1~	A3
C0:0	LCS0~	A1

Connections for 85XXLB_ADS Support Package

Tables 3–121 through 3–126 list the probe connections for the 85XXLB_ALT support package.

Table 3-121: Alternate Board Data connections

Logic analyzer channel	85XXLB_ADS support package signal name	TEK mictor pin number	AMP mictor pin number
Clock:0	LBCLK	3	5
A3:7	LAD0	4	7
A3:6	LAD1	5	9
A3:5	LAD2	6	11
A3:4	LAD3	7	13
A3:3	LAD4	8	15
A3:2	LAD5	9	17
A3:1	LAD6	10	19
A3:0	LAD7	11	21
A2:7	LAD8	12	23
A2:6	LAD9	13	25
A2:5	LAD10	14	27
A2:4	LAD11	15	29
A2:3	LAD12	16	31
A2:2	LAD13	17	33
A2:1	LAD14	18	35
A2:0	LAD15	19	37
Clock:1	LALE	36	6
A1:7	LAD16	35	8
A1:6	LAD17	34	10
A1:5	LAD18	33	12
A1:4	LAD19	32	14
A1:3	LAD20	31	16
A1:2	LAD21	30	18
A1:1	LAD22	29	20
A1:0	LAD23	28	22
A0:7	LAD24	27	24
A0:6	LAD25	26	26
A0:5	LAD26	25	28
A0:4	LAD27	24	30
A0:3	LAD28	23	32

Table 3-121: Alternate Board Data connections (Cont.)

Logic analyzer channel	85XXLB_ADS support package signal name	TEK mictor pin number	AMP mictor pin number
A0:2	LAD29	22	34
A0:1	LAD30	21	36
A0:0	LAD31	20	38

Table 3-122: Alternate Board Control connections

Logic analyzer channel	85XXLB_ADS support package signal name	TEK mictor pin number	AMP mictor pin number
Clock:3	No Connection	3	5
C3:7	LBCTL	4	7
C3:6	LSDDQM3/LWE3~	5	9
C3:5	LSDDQM2/LWE2~	6	11
C3:4	LSDDQM1/LWE1~	7	13
C3:3	LSDDQM0/LWE0~	8	15
C3:2	MA27	9	17
C3:1	MA28	10	19
C3:0	MA29	11	21
C2:7	MA30	12	23
C2:6	MA31	13	25
C2:5	LSDAMUX/LGPL5	14	27
C2:4	LGPL4	15	29
C2:3	LSDCAS~/LGPL3	16	31
C2:2	LSDRAS~/LBOE~/LGPL2	17	33
C2:1	LSDWE~/LGPL1	18	35
C2:0	LSDA10/LGPL0	19	37
Clock:2	MDVAL	36	6
D1:7	MSRCID4	35	8
D1:6	MSRCID3	34	10
D1:5	MSRCID2	33	12
D1:4	MSRCID1	32	14
D1:3	MSRCID0	31	16
D1:2	No Connection	30	18

Table 3-122: Alternate Board Control connections (Cont.)

Logic analyzer channel	85XXLB_ADS support package signal name	TEK mictor pin number	AMP mictor pin number
D1:1	TRIG_OUT	29	20
D1:0	LCKE	28	22
D0:7	LCS7~	27	24
D0:6	LCS6~	26	26
D0:5	LCS5~	25	28
D0:4	LCS4~	24	30
D0:3	LCS3~	23	32
D0:2	LCS2~	22	34
D0:1	LCS1~	21	36
D0:0	LCS0~	20	38

Table 3–123 lists the P6860 probe connections for the 85XXLB_ADS support package.

Table 3-123: A3/A2 probe head assignment for 85XXLB_ADS support package

Logic analyzer channel	85XXLB_ADS support package signal name	P6860 probe pad number
Clock:0-	GND	A15
Clock:0+	LBCLK	A13
A3:7	LAD0	B12
A3:6	LAD1	B10
A3:5	LAD2	A12
A3:4	LAD3	A10
A3:3	LAD4	B9
A3:2	LAD5	B7
A3:1	LAD6	A9
A3:0	LAD7	A7
A2:7	LAD8	B6
A2:6	LAD9	B4
A2:5	LAD10	A6
A2:4	LAD11	A4
A2:3	LAD12	B3

Table 3-123: A3/A2 probe head assignment for 85XXLB_ADS support package (Cont.)

Logic analyzer channel	85XXLB_ADS support package signal name	P6860 probe pad number
A2:2	LAD13	B1
A2:1	LAD14	A3
A2:0	LAD15	A1

Table 3–124 lists the P6860 probe connections for the 85XXLB_ADS support package.

Table 3-124: A1/A0 probe head assignment for 85XXLB_ADS support package

Logic analyzer channel	85XXLB_ADS support package signal name	P6860 probe pad number
Clock:1-	GND	A15
Clock:1+	LALE	A13
A1:7	LAD16	B12
A1:6	LAD17	B10
A1:5	LAD18	A12
A1:4	LAD19	A10
A1:3	LAD20	B9
A1:2	LAD21	B7
A1:1	LAD22	A9
A1:0	LAD23	A7
A0:7	LAD24	B6
A0:6	LAD25	B4
A0:5	LAD26	A6
A0:4	LAD27	A4
A0:3	LAD28	B3
A0:2	LAD29	B1
A0:1	LAD30	A3
A0:0	LAD31	A1

Table 3–125 lists the P6860 probe connections for the 85XXLB_ADS support package.

Table 3-125: C3/C2 probe head assignment for 85XXLB_ADS support package

Logic analyzer channel	85XXLB_ADS support package signal name	P6860 probe pad number
Clock:3-	GND	A15
Clock:3+	No Connection	A13
C3:7	LBCTL	B12
C3:6	LSDDQM3/LWE3~	B10
C3:5	LSDDQM2/LWE2~	A12
C3:4	LSDDQM1/LWE1~	A10
C3:3	LSDDQM0/LWE0~	B9
C3:2	MA27	B7
C3:1	MA28	A9
C3:0	MA29	A7
C2:7	MA30	B6
C2:6	MA31	B4
C2:5	LSDAMUX/LGPL5	A6
C2:4	LGPL4	A4
C2:3	LSDCAS~/LGPL3	B3
C2:2	LSDRAS~/LBOE~/LGPL2	B1
C2:1	LSDWE~/LGPL1	A3
C2:0	LSDA10/LGPL0	A1

Table 3–126 lists the P6860 probe connections for the 85XXLB_ADS support package.

Table 3-126: D1/D0 probe head assignment for 85XXLB_ADS support package

Logic analyzer channel	85XXLB_ADS support package signal name	P6860 probe pad number
Clk2-	GND	A15
Clk2+	MDVAL	A13
D1:7	MSRCID4	B12
D1:6	MSRCID3	B10
D1:5	MSRCID2	A12
D1:4	MSRCID1	A10
D1:3	MSRCID0	B9
D1:2	No Connection	B7
D1:1	TRIG_OUT	A9
D1:0	LCKE	A7
D0:7	LCS7~	B6
D0:6	LCS6~	B4
D0:5	LCS5~	A6
D0:4	LCS4~	A4
D0:3	LCS3~	B3
D0:2	LCS2~	B1
D0:1	LCS1~	A3
D0:0	LCS0~	A1

Signal Acquisition

This section shows the timing diagrams and tables that list details about how to acquire the relevant address and data from the 85XX local bus interface and DDR SDRAM interface.

Figure 3-8 shows signal acquisition for 85XXLB, 85XXLB_ALT, and 85XXLB_ADS support packages.

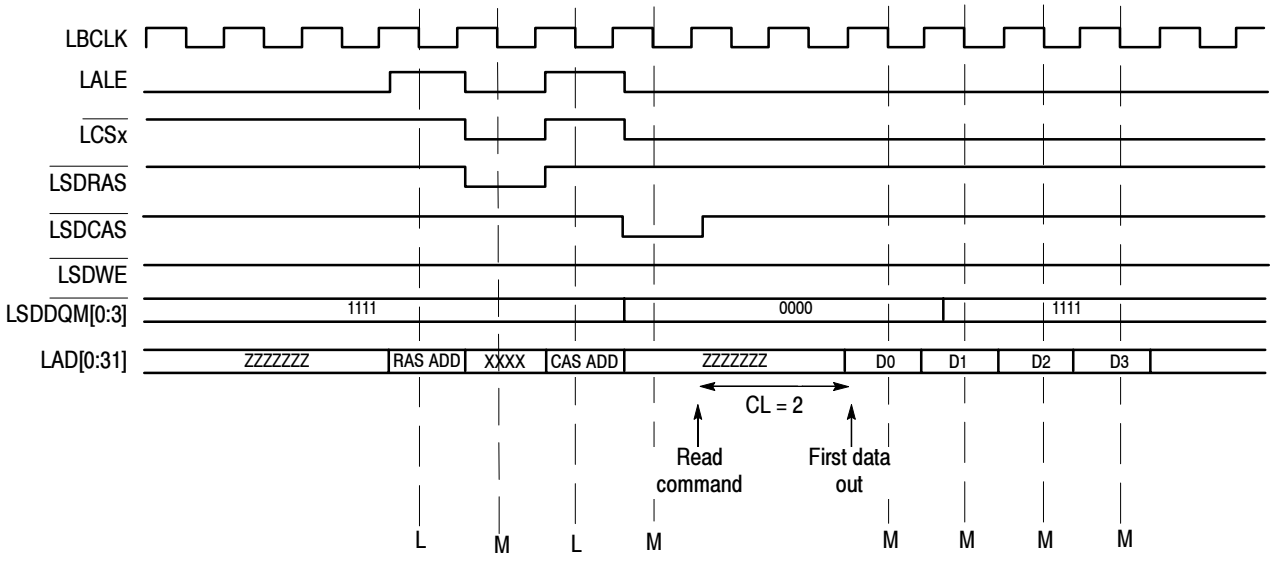


Figure 3-8: Timing diagram for Local bus interface

Table 3–127 illustrates the sample points for 85XXLB and 85XXLB_ADS support packages.

Table 3–127: Sample points for 85XXLB, and 85XXLB_ADS support packages

Master point	Signals
Master sample point, M	No signals
Sample point, Addr	LALE, LAD[0-31], LA[27-31], MSRCID[0-4]
Sample point, Control	LAD[0-31], LA[27-31], MDVAL, LSDDQM[0-3]/LWE[0-3]~, LGTA~, LBCTL, LSDA10/LGPL0, LALE, LSDRAS~/LBOE~, LSDCAS~/LGPL3, LSDWE~/LGPL1, LCS[0-7]~, MSRCID[0-4], LGPL5, LDP0/LCKE, LDP1/TRIG_IN, LDP2/TRIG_OUT, LDP3

Table 3–128 illustrates the sample points for 85XXLB_ALT support package.

Table 3–128: Sample points for 85XXLB_ALT support package

Master point	Signals
Master sample point, M	No signals
Sample point, Addr	LALE, LA_D[0-31], LA[27-31], MSRCID[0-4]
Sample point, Control	LA_D[0-31], LA[27-31], MDVAL, LSDDQM[0-3]/LWE[0-3]~, LGTA~, LBCTL, LSDA10/LGPL0, LALE, LSDRAS~/LBOE~, LSDCAS~/LGPL3, LSDWE~/LGPL1, LCS[0-7]~, MSRCID[0-4], LGPL5, LDP0/LCKE, LDP1/TRIG_IN, LDP2/TRIG_OUT, LDP3

Table 3–129 illustrates how the signals are stored based on the qualifier levels incase of 85XXLB, 85XXLB_ALT, and 85XXLB_ADS support packages.

Table 3-129: Signal accquisition for 85XXLB, 85XXLB_ALT, and 85XXLB_ADS support packages

Qualifiers	Operation	Master point	Signals
LALE = HIGH & LSDRAS~/LBOE~ =HIGH	Addr	LALE, LA_D[0-31], LA[27-31], MSRCID[0-4]	Log address as long as LALE is asserted
LSDRAS~/LBOE~ = LOW LSDCAS~/LGPL3 = HIGH LSDWE~/LGPL1 =HIGH LALE = LOW (Activate) OR LSDRAS~/LBOE~ = LOW LSDCAS~/LGPL3 = HIGH LSDWE~/LGPL1 = LOW LALE = LOW (Precharge) OR LSDRAS~/LBOE~ = LOW LSDCAS~/LGPL3 = LOW LSDWE~/LGPL1 = HIGH LALE=LOW (Refresh) OR LSDRAS~/LBOE~ = LOW LSDCAS~/LGPL3 = LOW LSDWE~/LGPL1 = LOW LALE=LOW (MRS) OR LSDRAS~/LBOE~ = HIGH LSDCAS~/LGPL3 = LOW LSDWE~/LGPL1 = HIGH LALE=LOW (Read) OR LSDRAS~/LBOE~ = HIGH LSDCAS~/LGPL3 = LOW LSDWE~/LGPL1 = LOW LALE=LOW (Write) OR LALE = LOW LSDRAS~/LBOE~ = HIGH	Control, M	LAD[0-31], LA[27-31], MDVAL, LSDDQM[0-3]/LWE[0-3]~, LGTA~, LBCTL, LSDA10/LGPL0, LALE, LSDRAS~/LBOE~, LSDCAS~/LGPL3, LSDWE~/LGPL1, LCS[0-7]~, MSRCID[0-4], LGPL5, LDP0/LCKE, LDP1/TRIG_IN, LDP2/TRIG_OUT, LDP3	This operation saves the address and the SDRAM commands (if any)

If there is no valid SDRAM command after LALE is negated the support assumes GPCM transactions and saves next 6-clock information.

Figure 3-9 shows the timing diagram for DDR SDRAM interface.

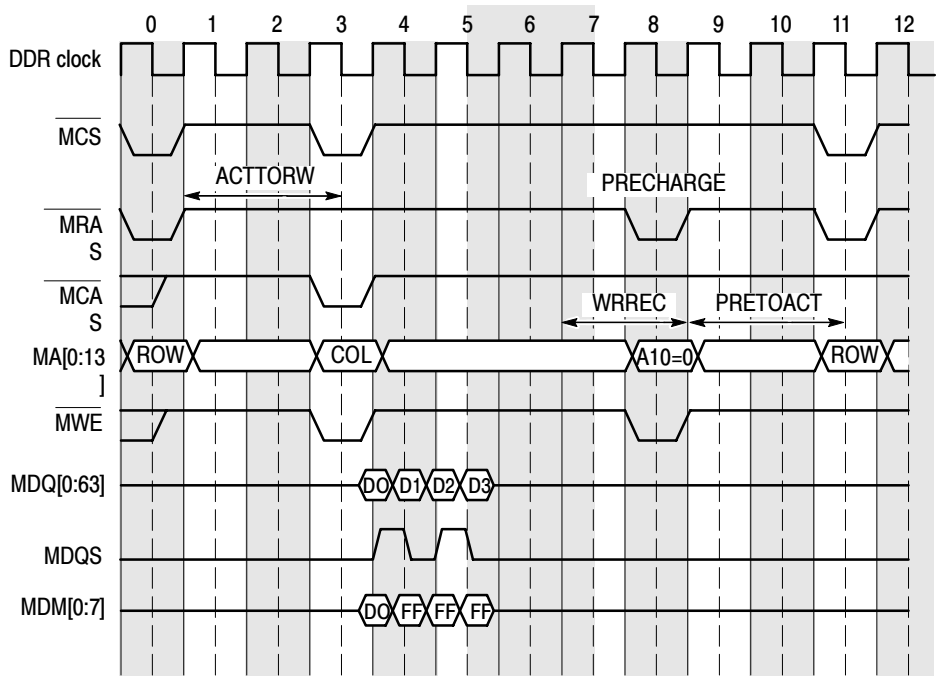


Figure 3-9: Timing diagram for DDR SDRAM interface

Table 3-130 illustrates the sample points for 85XXDDR and 85XXDDR_RW support packages.

Table 3-130: Sample points for 85XXDDR and 85XXDDR_RW support packages

Sample point	Signals
Master Sample Point, M	All signals

Table 3–131 illustrates the signal acquisition for 85XXDDR and 85XXDDR_RW support packages.

Table 3–131: Signal acquisition in 85XXDDR and 85XXDDR_RW support packages

Qualifiers	Operation	Signals	Description
MRAS~ = LOW MCAS~ = LOWWE~=LOW	M	All signals	MRS cycle
MRAS~ = LOW MCAS~ = HIGHWE~=HIGH	M	All signals	Row Address
MRAS~ = LOW MCAS~ = LOWWE~=HIGH	M	All signals	Refresh cycle
MRAS~ = HIGHMCAS~ = LOWWE~=HIGH	M	All signals	Read cycle
MRAS~ = HIGH MCAS~ = LOWWE~=LOW	M	All signals	Write cycle

85XXDDR and 85XXDDR_RW samples 16-clock edge information on all channels after above valid commands are issued.

Specifications

Specifications

This section contains the specifications for the TMS568 MPC85XX microprocessor support product.

Specifications Table

Table 4–1 lists the electrical requirements that the target system must produce for the support to acquire correct data.

Table 4–1: Electrical specifications

Characteristics	Requirements
Target system clock rate	
MPC85XX specified clock rate	[1]The maximum rates are 166 MHz for local bus SDRAM and 200 MHz for DDR-SDRAM depending upon the type of logic analyzer module
Minimum setup time required for the	
Logic analyzer TLA7Axx	0.750 ns
Minimum hold time required for the	
Logic analyzer TLA7Axx	0 ns
Minimum setup time required for the	
Logic analyzer TLA7xx	2.5 ns
Minimum hold time required for the	
Logic analyzer TLA7xx	0 ns

[1] **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest bus supported.**

Replaceable Parts List

Replaceable Parts List

This section contains a list of the replaceable components and modules for the MPC85XX product. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Parts List

The tabular information in the *Replaceable Parts List* is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Parts List.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX, INC.	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR, 97077-0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071-1191-XX			1	MANUAL,TECH INSTRUCTION	80009	071-1191-XX

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